**Layout Guidelines**

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1) **Orientation of Vdd/Gnd lines in schematics**

For no good reason other than to choose a convention that follows circuit schematics with Vdd (higher voltage) on top and Gnd (lower voltage) on bottom, normally route Vdd and Gnd as shown.

2) **Stacking transistors**

Straightforward method:

Ex: 

<table>
<thead>
<tr>
<th>Gnd</th>
</tr>
</thead>
</table>

It is much better to **share diffusion**— in this case across two NMOS transistors, mainly because of smaller area:

| Gnd |

= Normally do it this way.
3) Orientation of transistors

“Vertical” transistors:
+ short poly
+ easy to stack many transistors
(generally done like this)

Horizontal transistors:
- limited room to stack transistors
- long poly
+ easier to make wide transistors
4) Routing of Vdd/Gnd
- In Metal (probably never in poly, diff. only for short distances
  - **Metal 1**
    - +very convenient
    - Most commonly used
  - **Metal 2**
    - +signals can go under power rails easily
  - Use thicker wires to route power (6λ+), large (many) contacts

5) Rows of diffusion in a cell
- **Two**:  
  - Preferable
- **Four**:  
  - Often leads to big empty spaces
  - +Can be easier to fit large complex cells
  - -Doesn't work well with a standard cell height
    - Generally avoid if possible
6) Cell Placement
- Key idea: line up and share Vdd and Gnd
- This requires that every other row is flipped, with Gnd on the top, and Vdd on the bottom

7) Metal routing discipline
- Suppose we need to route across this example cell, we would have to via all the way up to Metal 5!
- Key point: every wire blocks perpendicular wires from using that layer

a) Guideline: try to use only M1 and M2 in small cells
b) Guideline: Use only one direction for each layer

Ex (bad!):

Ex (good!):

c) Guideline: Alternate directions with each layer
Ex: Horizontal: (M1), M3, M5
Vertical: (M2), M4, M6
Exception: generally ok to route M1 and M2 any direction inside a cell to keep area small, then we just need to use M3+ to route over a cell

d) Guideline: use lower level metals for short wires, and higher level metals for longer wires

Ex (side view):

e) Guideline: try to minimize vias (metal layer changes), as they are highly resistive
-When possible
8) Stack vias to reduce area
   • With older technology this wasn’t possible
   • Now, thanks to CMP, vias can be stacked
   • Most advanced processes can stack arbitrarily high
   • In our Magic however:

9) Reduce area
   a) Share, overlap

   b) Abut

   c) Avoid wires that turn corners, if possible
      i) A
      ii) A
      iii) A
      iv) A

"pitch matching" – Try to pitch the cells that are going to abut to be the same size as each other if possible
d) Consider shape of overall structure

Ex, full adder chain:

For an arbitrary block, a square will give the shortest total wire length

Better:

• Large source and drain caps.
• With very large transistors, we will not be able to fit this inside a allotted cell height

Better:

• Source cap. is larger (good)
• Drain cap. is reduced (good)

e) Transistor folding (for large devices)

10) Reduce maximum delay

\[ t_p = 0.69 \cdot R_{MOS} \cdot C_L \]

• Reduce \( R_{MOS} \)
  • In layout, this means wider transistors, but this increases load cap.
  for draining gate, helps a lot for under-driven nets, diminishing returns eventually
• Reduce \( C_L \)
  • Shorter wires \( \Rightarrow \) smaller area \( \Rightarrow \) lower \( C_L \) \( \Rightarrow \) reduce MOS widths \( \Rightarrow \) smaller area ...
  • Use higher-level metals if possible

11) Reduce power

\[ P = C_L V^2 f \]

• Reduce \( C_L \)
• Vdd and f are generally set by other requirements
• Other more complex techniques are possible

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