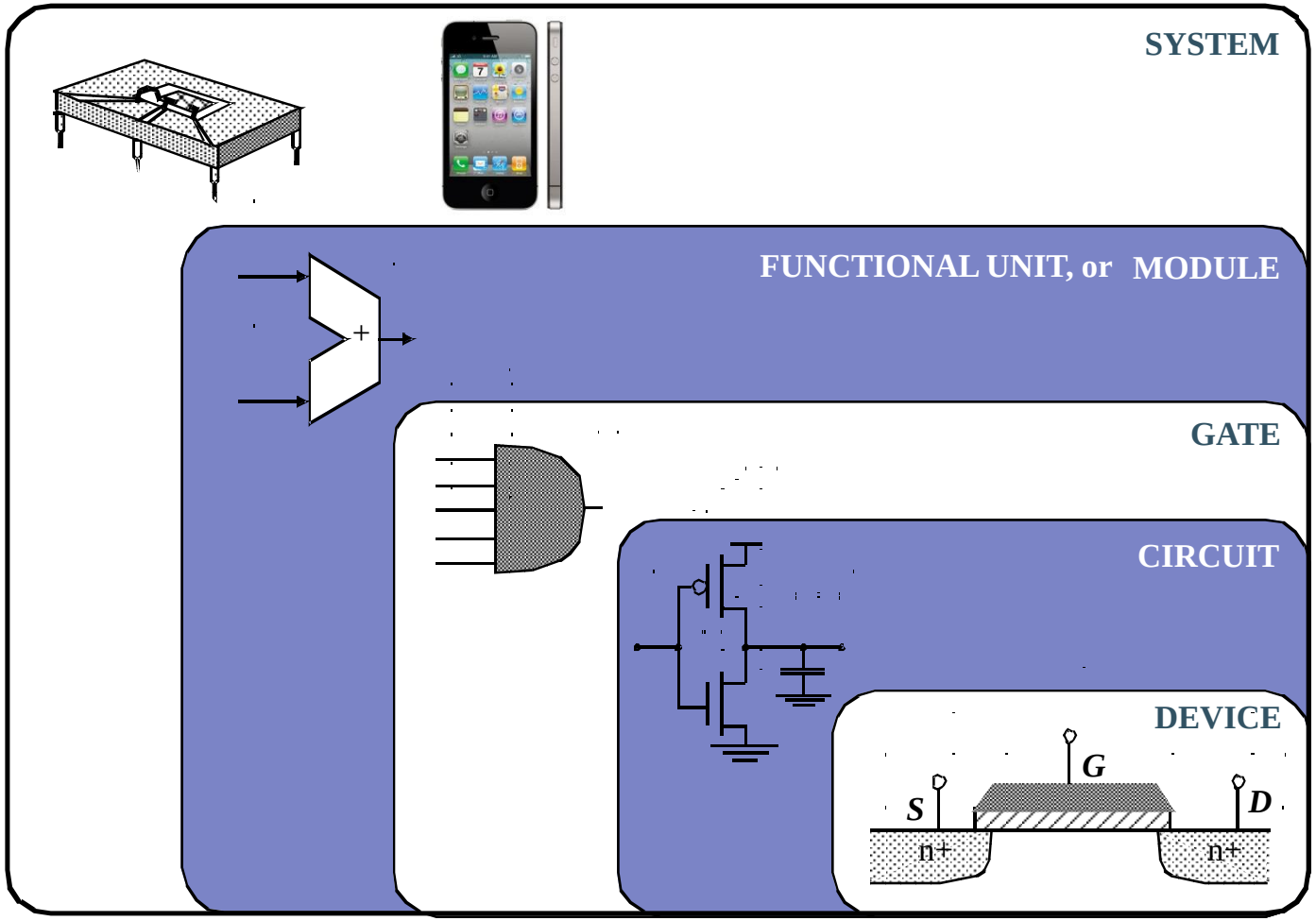
ABSTRACTION OF COMPLEXITY

Abstraction of Design Complexity

- Design complexity
  - Typically tens of transistors in analog circuits
    - Each is normally hand crafted along with placement and wiring
  - Hundreds of transistors
    - Each can be hand crafted
  - Thousands to 100s of thousands of transistors
    - Must find regularity in structure and exploit it (re-use cells)
    - Ex: memory
  - Millions to billions of transistors
    - Must find high-level regularity in structure and exploit it (re-use modules and subsystems)
    - Ex: System on Chip (SOC)

Design Abstraction Levels

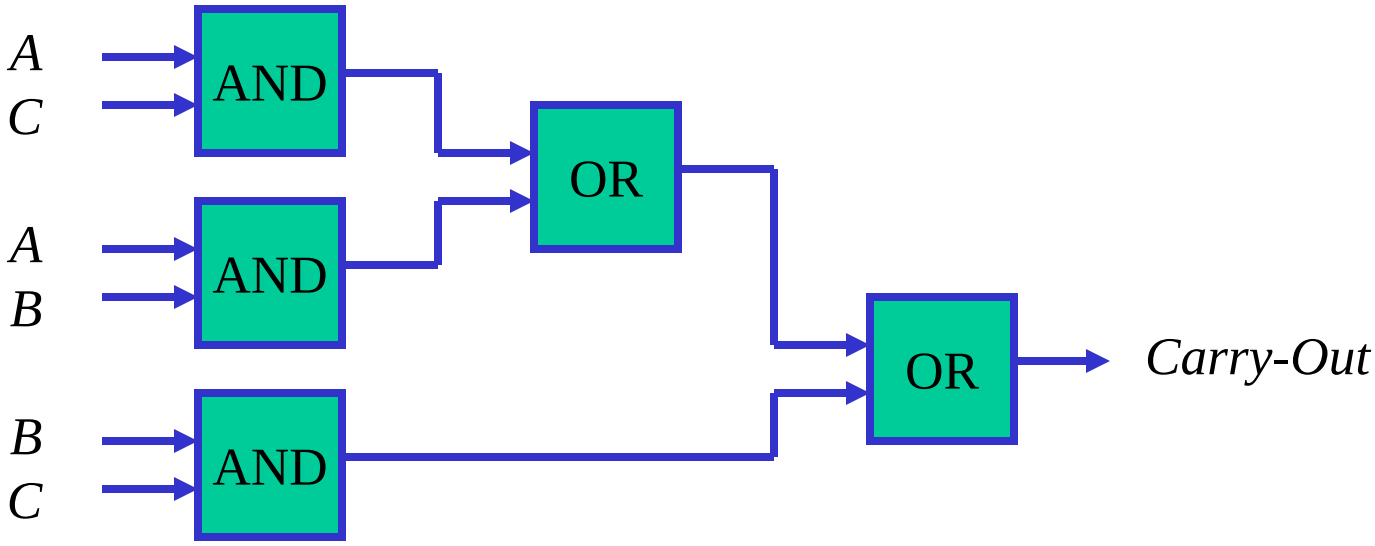


Abstraction of Design Complexity

- Levels
  - Devices and Wires
  - Circuits, for example simulated by Spice
  - Gates, for example simulated by a digital simulator
  - Modules and functional units (e.g., adder, memory, etc.)
  - Sub-systems (e.g., processor, display driver, network interface, etc.)
- Methods to *abstract* complexity
  - Sophisticated Computer-Aided-Design (CAD) tools
  - Standard cell libraries

Hierarchical Abstraction

- Example: While designing at the gate level, we do not consider the circuit inside each gate



Why Should We Learn About Circuits and Layout Then?

- The best designers can:
  - Build model abstractions
  - Understand limitations of models
    - Wire or interconnect performance
    - Changes with technology scaling
- Abstractions limit maximum attainable performance and energy-efficiency
  - Multi-disciplinary view needed
- Troubleshooting
  - Malfunctions are often at interfaces:
    - Interfaces between modules
    - Unexpected interactions between levels of abstraction; e.g., an abstracted module was used in a way never anticipated

Examples of Design Aspects that "Defy Hierarchy"

- Clock distribution
  - Skew in the timing of active clock edges between different clock signals
  - Worst case result: unfixable faults due to signals passing through two registers in one clock cycle
- Power distribution
  - Sufficient current handling is required for proper operation
  - Adequate noise suppression in the power and ground grids
  - Worst case result: unfixable faults due to power and ground grid droops resulting in outcomes such as:
    - Memory element erasure
    - Unacceptably slow performance (critical in real-time systems)