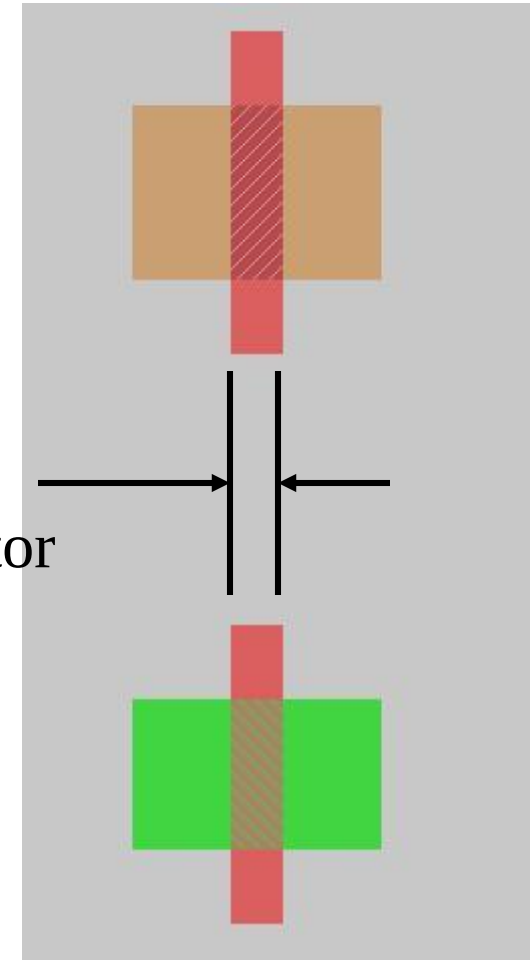
BASICS: TECHNOLOGIES

Minimum Feature Size

- Fabrication technologies (often called just *technologies*) are named after their minimum feature size—which is generally the minimum gate length
- For example, 0.13 μm where 1 μm
  = 1 micrometer
  = 1 10^{-6} m
  = 1 "micron"
  = 1000 nanometers



"top" view

Major Technology Nodes

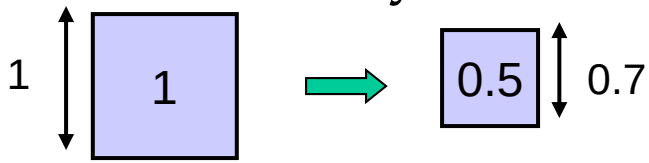
- Mostly just the primary representative technology nodes with sqrt(2) scaling are shown. Others exist, e.g. 40 nm
- Area scaling assumes perfect scaling with the minimum feature size which is only approximate

DSM = Deep Sub-micron

Technology	Approx. Year	Relative Area
1.00 µm	1986	256
0.70 µm	1989	128
0.50 µm	1991	64
0.35 µm	1994	32
0.25 µm	1998	16
0.18 µm	2000	8
0.13 µm	2002	4
90 nm	2004	2
65 nm	2006	1
45 nm	2007 H2	0.5
32 nm	2010 H1	0.25
22 nm	Aug 2010 24 nm Toshiba flash	0.13
16 nm	~2013	0.063
14 nm	Jan 2015, Intel i7	0.046
11 nm	2017?	0.031
5-10 nm?	?	-

Technology Scaling

- Linear dimension shrinks by 0.7x/technology generation



- Every generation can integrate 2x more functions per chip
  - Chip cost does not increase significantly
  - → Cost of a function decreases by 2x each generation
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Challenges in DSM Digital Design

∝ Min. Feat. Size

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution

∝ 1/(Min. Feat. Size)

"Macroscopic Issues"

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.