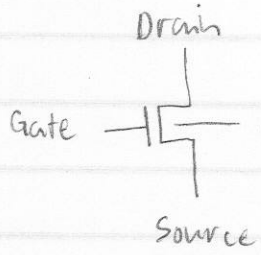
Chapter 3 – MOSFET R, C, latchup, and scaling

MOSFETs have 4 terminals



(review)

In common operation, we care most about:

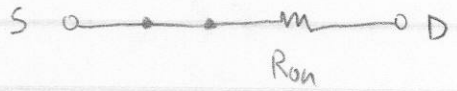
input: gate voltage (V_G or V_{GS})

output: source-drain current (I_D)

MOSFET switch model:

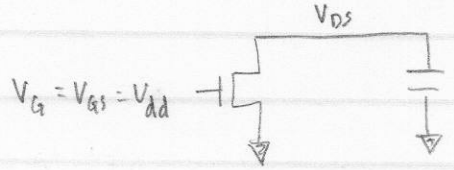
If $V_{GS} < V_T$, $\rightarrow$ $I_D \sim 0$ ($I_{LEAKAGE}$ only), where V_T = "threshold" voltage

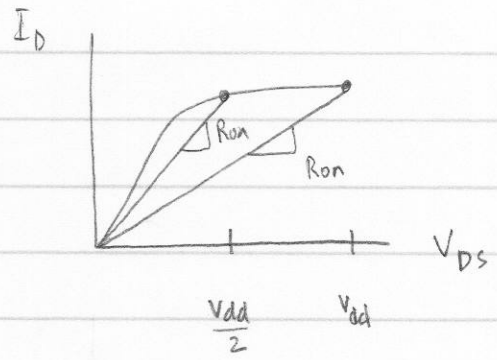
If $V_{GS} \geq V_T$, $\rightarrow$ $I_D = \frac{V_{DS}}{R_{on}}$ (transistor "on")



I. MOSFET Resistance

But in a real transistor, Ron changes while switching





For speed purposes, we care about region where V_{DS} (output) goes from V_{dd} to $V_{dd}/2$.

Resistance Ron at these points is slope of lines through operating point and origin.

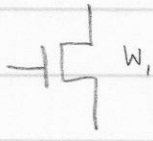
$$R_{on} = \frac{V_{DS}}{I_D}$$

switch-level

For our simulator for extracted layout (irsim) we will choose Ron by simulations so that delays closely match spice.

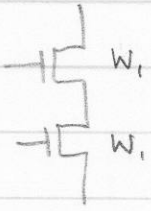
Ron is proportional to $\frac{\text{Transistor channel length}}{\text{Transistor channel width}} = \frac{L}{W} = \frac{1}{W/L}$

a)



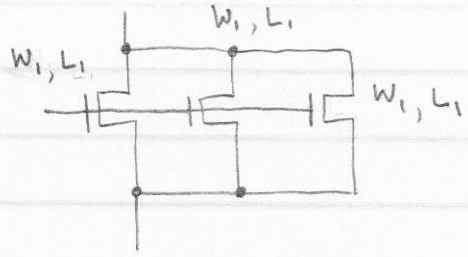
$$R_1 = K \frac{L_1}{W_1}$$

b)



$$R = K \frac{L_1 + L_1}{W_1} = 2R_1$$

c)



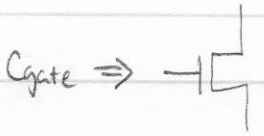
$$R = K \frac{L_1}{W_1 + W_1 + W_1} = \frac{R_1}{3}$$

Typical Ron values: (p. 106) For 0.25 μm with W=L = 0.25 μm

	Vdd			
	1V	1.5V	2V	2.5V
NMOS	35 KΩ	19 KΩ	15 KΩ	13 KΩ
PMOS	115	55	38	31

II. MOSFET Capacitance

A) Gate capacitance

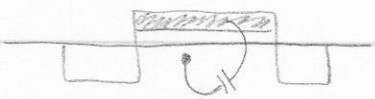


Large component of load capacitance for circuits

Typical value for 0.25 μm :

$C_{ox} = 6\ fF/\mu m^2$ for NMOS and PMOS

i)

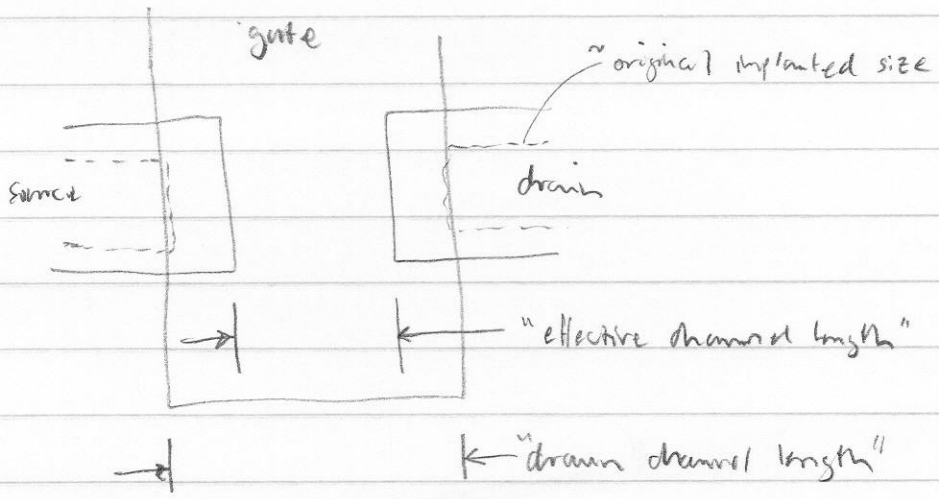


Bottom of gate to channel

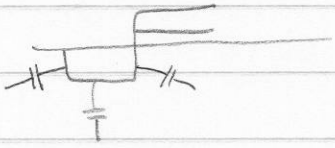
ii)

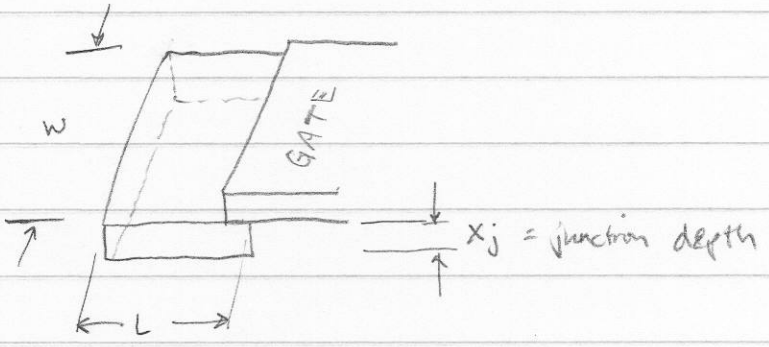
Sides of gate to Source and Drain

iii) Overlap capacitance: gate to source/drain:



B) Junction capacitances





- sidewall - area cap. of sides of junctions

- $C_{sw} = C'_{jsw}$ · sidewall area (3 sides only!)
  $= C_{jsw} \cdot x_j \cdot$ sidewall perimeter (" ")

- bottom plate - area cap. of bottom of junctions

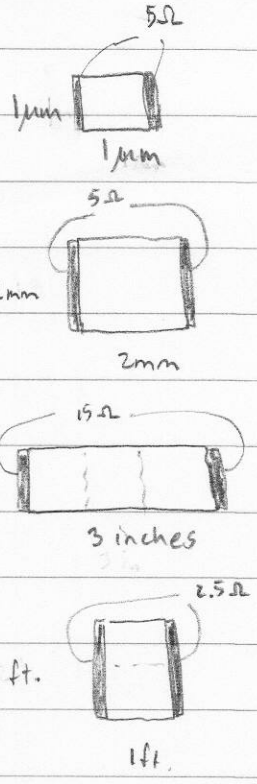
$C_{bottom} = C_j^{bottom} \times$ area

III. Resistance of materials

Sheet resistance - units of $\Omega/\square$ = Ω/ square.

Resistivity and depth assumed constant

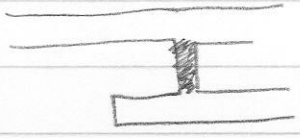
Ex. 5 $\Omega/\square$ material



Typical values 0.18μm CMOS

7 $\Omega/\square$	N+
8 $\Omega/\square$	P+
8 $\Omega/\square$	poly
2K $\Omega/\square$	poly without silicide
1K $\Omega/\square$	nwell
0.1 $\Omega/\square$	metal
0.05 $\Omega/\square$	top metal (m6) (double-thick)

IV. Contact resistance



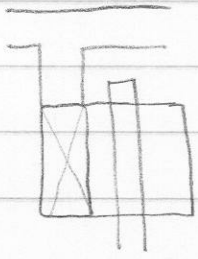
Aluminum or Tungsten

Typical 0.18 μm :

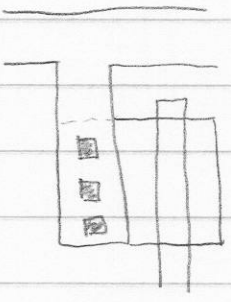
11 Ω	N+ - M1	Silicon to metal
11 Ω	P+ - M1	
10 Ω	poly - M1	
5 Ω	M1 - M2	

for each contact

In magic,



In mask,



So use large contacts in a real chip if there is room or if there are high currents