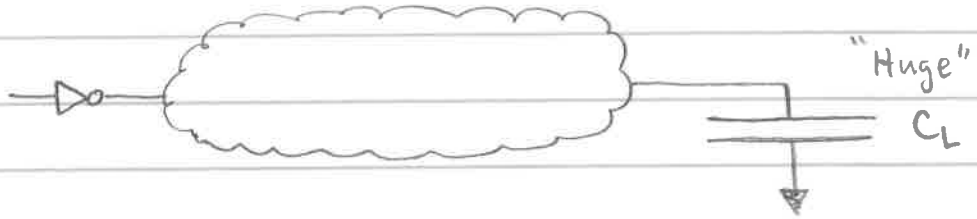
"Chain of Inverters" problem:

What circuit will drive a large load with the smallest delay?



First, some background:

C_g = input gate capacitance

C_{int} = intrinsic output capacitance (mostly diffusion cap.)

C_{ext} = cap. external to inverter (wire + load)

$$C_{int} = \gamma C_g \qquad \text{"gamma"}$$

$\gamma \simeq 1$ for modern processes, and is a function of technology

f = "effective fanout"

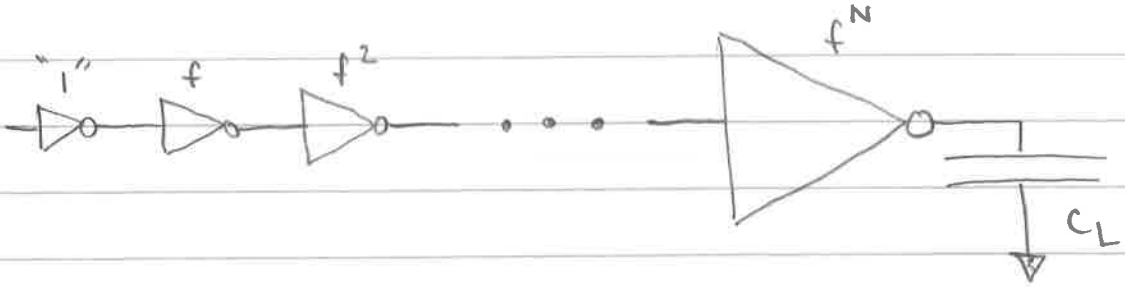
$$= C_{ext} / C_g$$

$$t_p = t_{p_0} + t_{p_0} \frac{f}{\gamma}$$

= function of f only! [Key point]

$$\frac{f}{\gamma} = \frac{C_{ext}/C_g}{C_{int}/C_g} = \frac{C_{ext}}{C_{int}}$$

Back to chain of inverters:



N = Number of stages

F = overall effective fanout

$= C_L / C_{g_1}$ $\quad C_{g_1}$ = C_g of first inverter

$f = \sqrt[N]{F}$ for a constant f across all stages

Choose number of stages (N) to minimize delay for a given F

$f = e^{(1+\gamma/f)}$

1) Assume $\gamma = 0$ → $C_{int} = 0$ simplification

$N = \ln(F)$ solved closed form

$f = e$

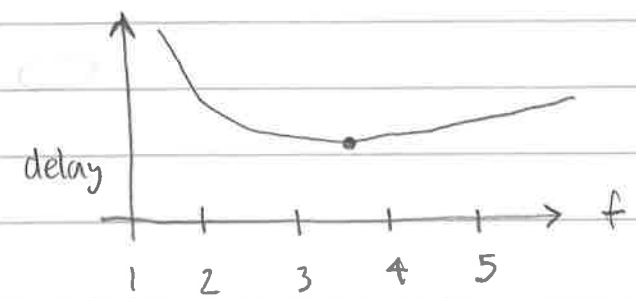
$= 2.72$

2) $\gamma = 1$ (more realistic)

$f = 3.6$ solved numerically book graphs

Optimum $f \simeq 3.6$. When that isn't possible, it is better to aim a little high rather than low.

- too low is very slow
- lower f → more gates

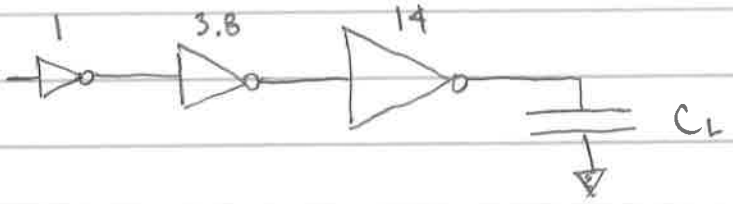


Ex: F = 50, neglect inversions, first inv has $W_p = 6\lambda$, $W_n = 4\lambda$

N = 2 : $\sqrt[2]{50} \simeq 7$

N = 3 : $\sqrt[3]{50} \simeq \boxed{3.8}$ ✓

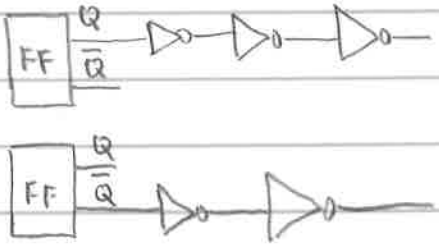
N = 4 : $\sqrt[4]{50} \simeq 2.8$



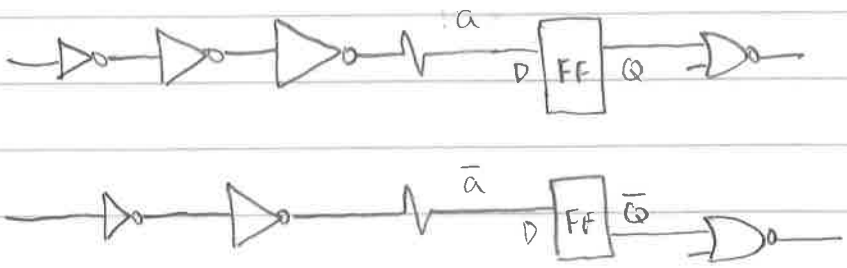
W_{PMOS}	6λ	23λ	84λ
W_{NMOS}	4λ	15λ	56λ

Of course if inversions are not negligible, we can choose only odd/even N value. Or:

a) Use $\bar{Q}$ FF output instead of Q:



b) DFF input too



c) absorb into logic