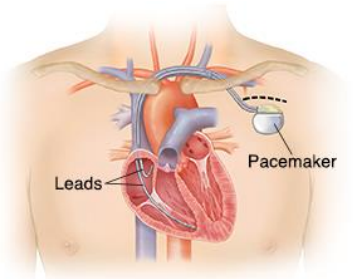
COST

Design Metrics

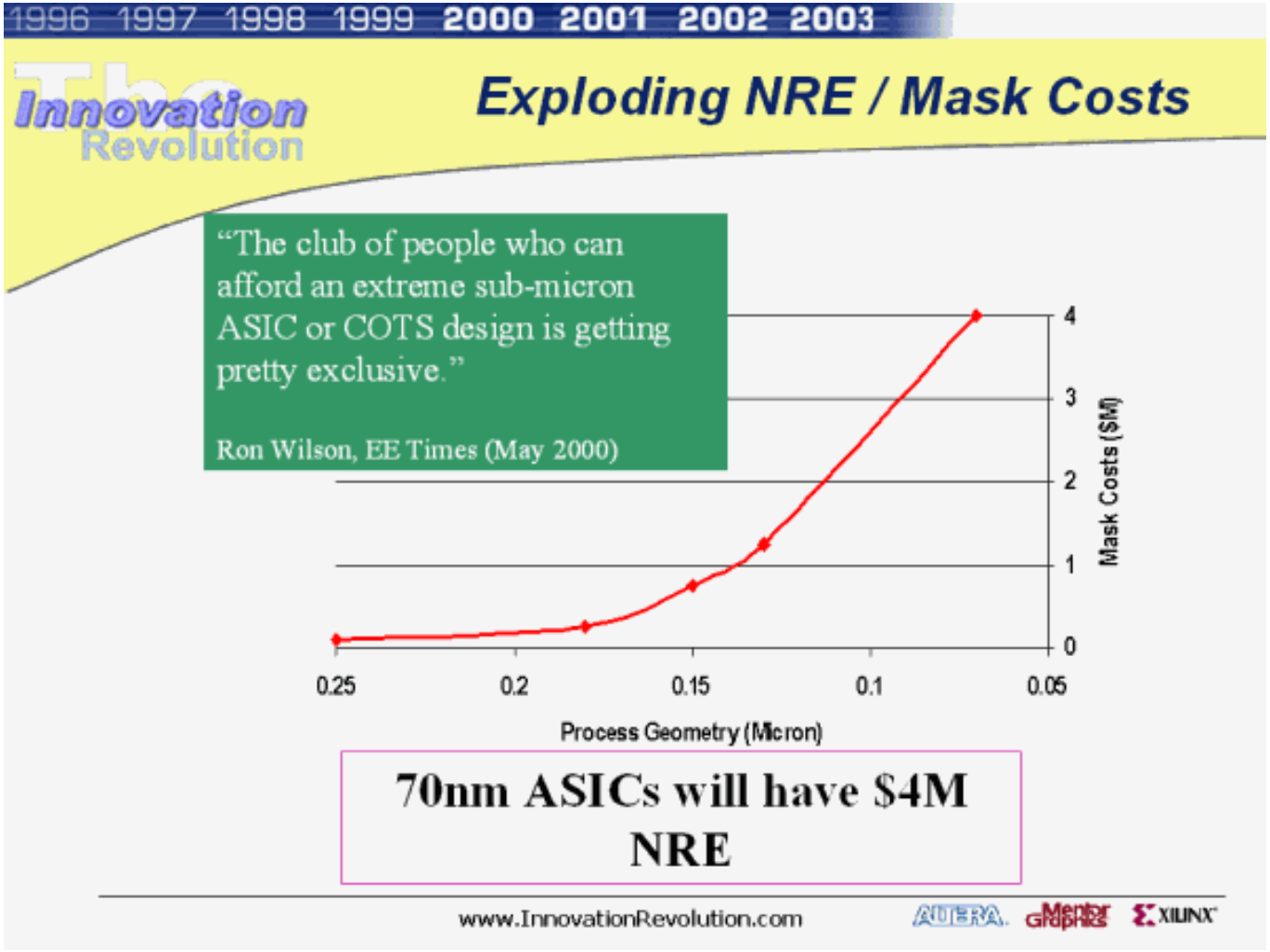
- Metrics to evaluate performance of a digital circuit (at any level; e.g. gate, block, …)
  - **Energy** to perform a function
  - **Performance** (clock maximum operating frequency, workload throughput, workload latency)
  - **Cost** (cost is a strong function of chip area)
  - **Design time**
  - Power dissipation (often peak power is of greatest concern)
  - Scalability
  - Reliability
- Relative cost depends on the application, for example:
  - Heart pacemaker (reliability, energy most important)
  - RFID (cost, energy most important)
  - PC graphics processor (speed most important)



Cost of Integrated Circuits

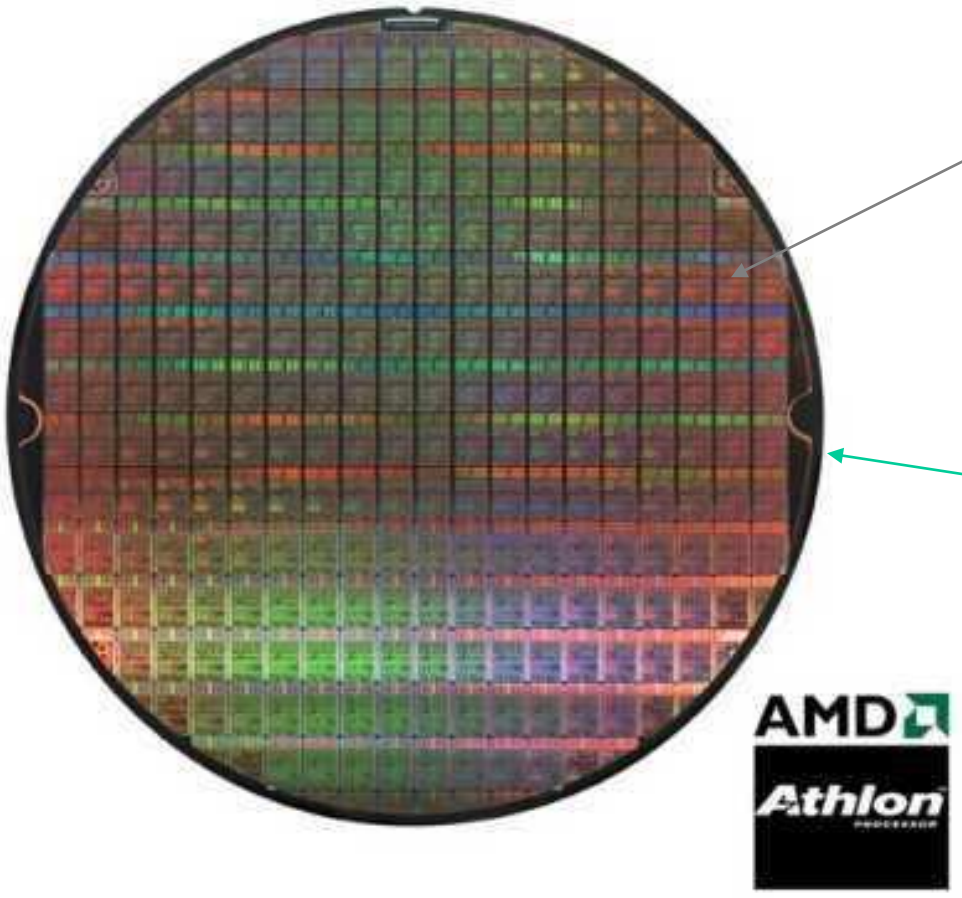
- cost/chip = fixed cost per design + variable cost per chip
  - Cost varies tremendously depending on the number of chips sold
- Fixed costs per design, NRE (non-recurrent engineering)
  - Design time and effort (designers and designer support)
  - Mask generation
  - CAD (computer aided design) software tools
  - Company costs (sales, marketing, building,…)
- Recurrent costs are costs for each chip
  - Some cost reductions with higher volumes
  - Silicon processing
    - Cost is strongly tied to chip area
  - Chip packaging and test

NRE Cost is Increasing



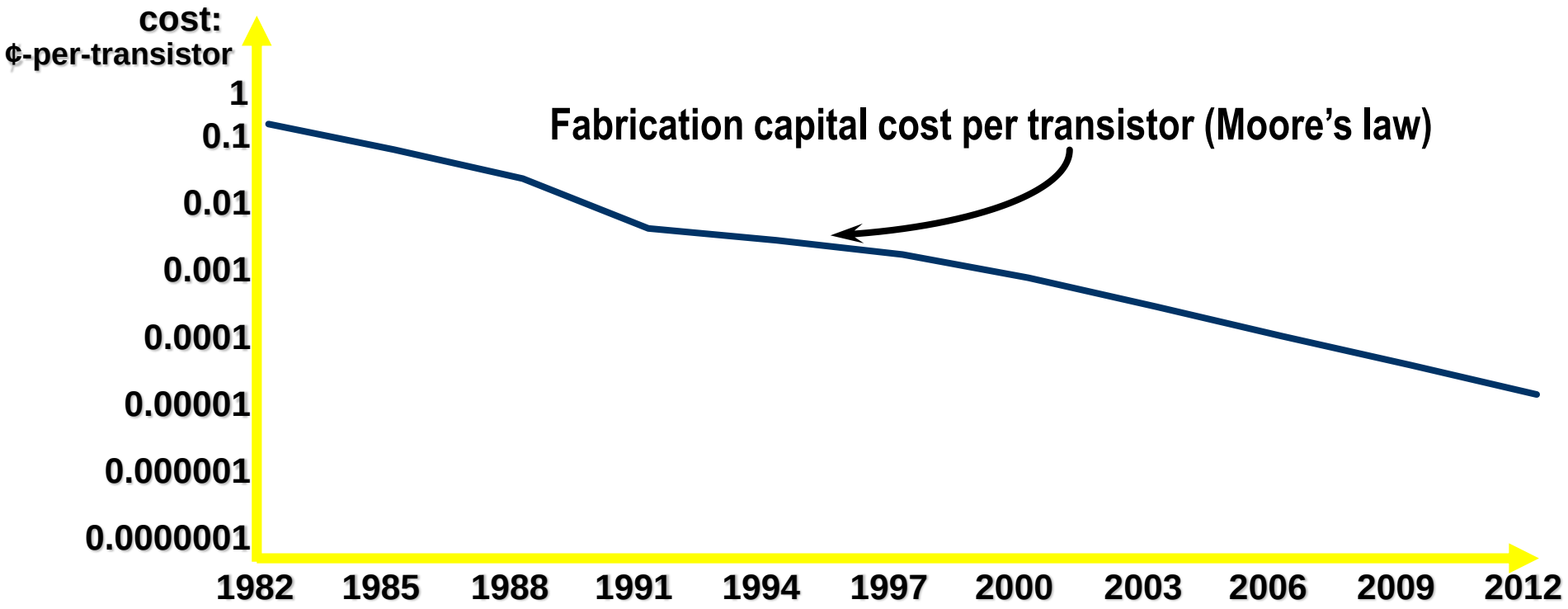
Modern ASICs (Application-Specific Integrated Circuits) are said to cost on the order of $50 million to design and require 18 to 24 months of effort by a large and talented design team [ITRS 2009]

Die Cost

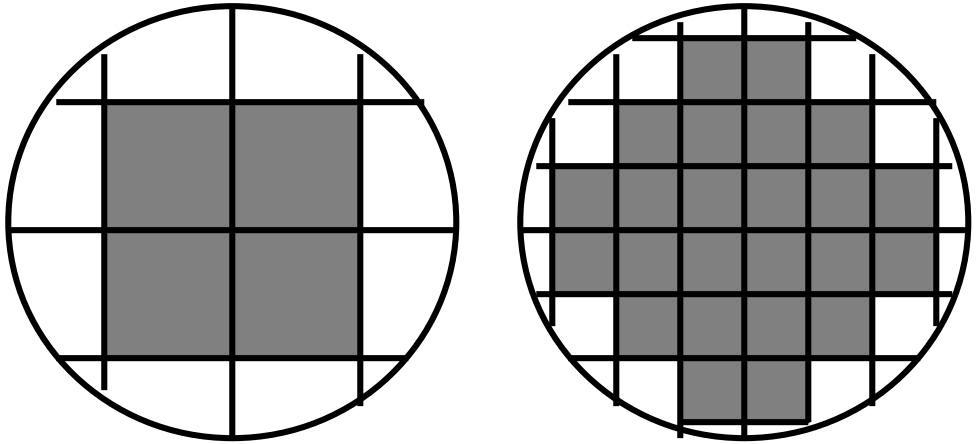


Source: http://www.amd.com

Cost per Transistor

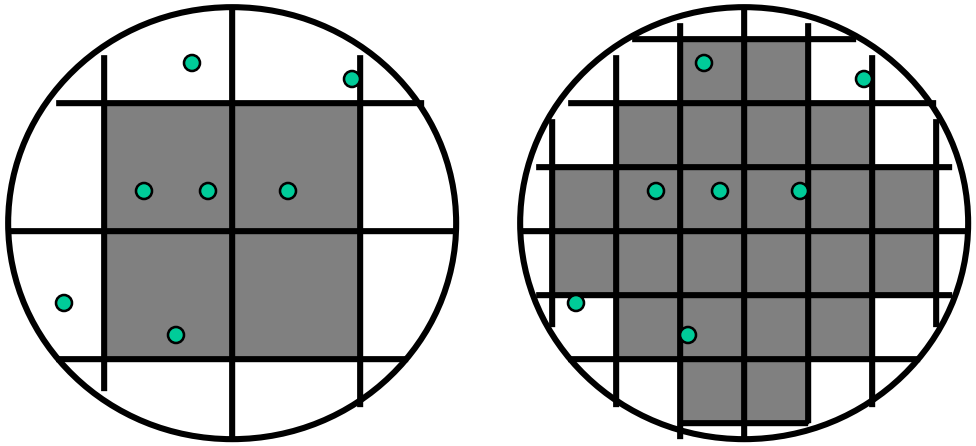


Area Equations



$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

Defects



$$DieYield = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$DieYield = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

Defects

- Alpha is roughly proportional to the number of "mask layers" (discussed next lecture)
- Alpha = 3 approximately for modern CMOS processes
- 0.5 – 1 defects/cm^2 typical for modern CMOS process

$$DieCost = \frac{WaferCost}{NumGoodDiesPerWafer}$$

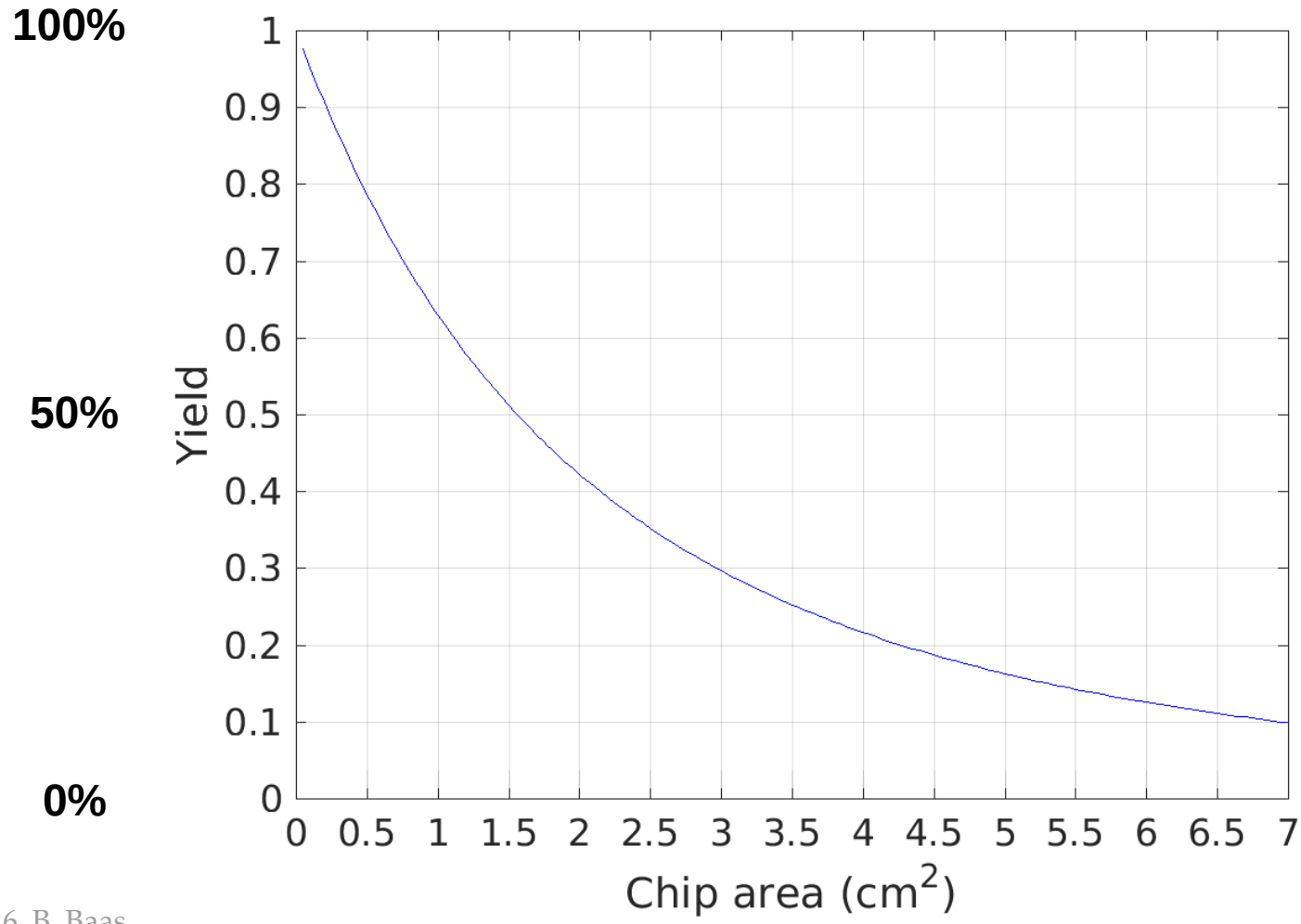
$$DieCost = \frac{\text{WaferCost}}{\text{Dies per wafer} \times \text{DieYield}}$$

$$DieCost = f(DieArea^4)$$

Some Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	**$4**
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	**$53**
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	**$417**

Matlab Example
Die Yields with *alpha*=3, 0.5 defects/cm^2



Example Matlab Code to Plot Yield vs. Chip Size

```
% Chip yield plot generator
%
% 2019/10/09  Updated (BB)
%
% Copy & paste this code into a example.m file and try it yourself!

clear;
alpha   = 3;
defects = 0.5;                              % 0.5 defects/cm^2
alimits = 0.05:0.05:7;

for x = alimits*20,
   x = round(x);                            % remove VERY small roundoff errors
   a = alimits(x);                          % die area
   y1(x) = (1+defects*a/alpha)^-alpha;      % "original" size die: blue
end

clf;
plot(alimits, y1, 'b');
hold on;
xlabel('Chip area (cm^2)');
ylabel('Yield');
set(gca,'XTick',[0:0.5:7])                  % prints X tick marks every 0.5
set(gca,'YTick',[0:0.1:1])                  % prints Y tick marks every 0.1
%legend('Reference chip');
axis([0 max(alimits) 0 1]);
grid on;
set(gca,'FontSize',16)                      % sets font size of axis

disp('Die yields with alpha=3 and 0.5 defects/cm^2');

print -dtiff example.tiff
```