MOSIS

- Low-cost VLSI prototyping and small-volume production service
- Affiliated with Information Sciences Institute at USC in Marina del Rey, California
- Since 1981, they have fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions
- Traditionally has been best place for support of magic and design rules
  - Changing somewhat recently
- CMP provides same services, based in France

Design Rules

- Interface between designer and process (CMOS fabrication) engineer
- Guidelines for constructing fabrication masks
- Units commonly used
  - scalable design rules: lambda (λ) parameter (used in magic), or
  - absolute dimensions (micron rules)
- Common rule examples:
  - minimum width
  - minimum separation same material
  - minimum separation different material
- Look for white dots in magic that show errors
Design Rules

- Mead and Conway, 1980
  - “Lambda-based” scalable design rules
  - Allows full-custom designs to be easily reused from technology generation to technology generation
  - Lambda is roughly one half the minimum feature size
    • “1.0 μm technology” ⇒ 1.0 μm min. length, \( \lambda = 0.5 \) μm
    • “0.5 μm technology” ⇒ 0.5 μm min. length, \( \lambda = 0.25 \) μm
  - For our class, we are using a 0.18 μm technology so lambda is 0.09 μm

- See course website for link to our scalable design rules on the MOSIS website
- We are using “SCMOS_DEEP” rules

Example Intra-Layer Design Rules

Source: Digital Integrated Circuits, 2nd ©
Example Design Rules: Transistor Layout

Example Design Rules: Vias and Contacts
In magic, white dots appear at the point of a DRC rule violation.

Place a box around white dots and press “y” to see what is causing an error.

Source: Digital Integrated Circuits, 2nd ©