Layout Guidelines

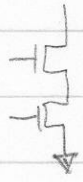
① Orientation of Vdd / Gnd like in schematics

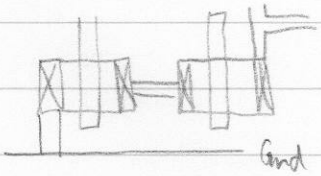
Vdd

Gnd

② Stacking transistors

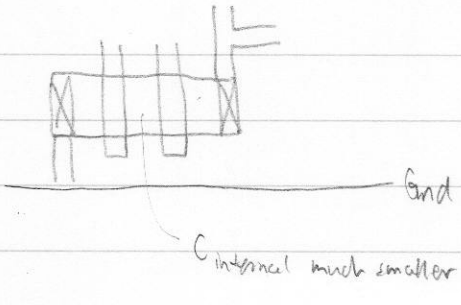
Ex:





Much better to "share diffusion"!

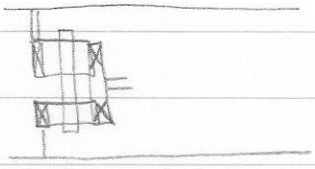
- Smaller area



③ Orientation of transistors

* transistors "vertical"

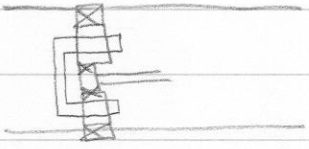
+ short poly



transistors "horizontal"

- limited room to stack transistors

+ easier to make wide transistors



B. Baas

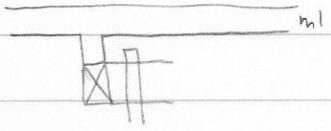
④ Routing of Vdd/Gnd

- In metal (poly probably never, diff. only for short distances)

* - metal 1

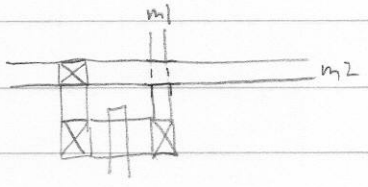
+ Very convenient

• most common



- metal 2

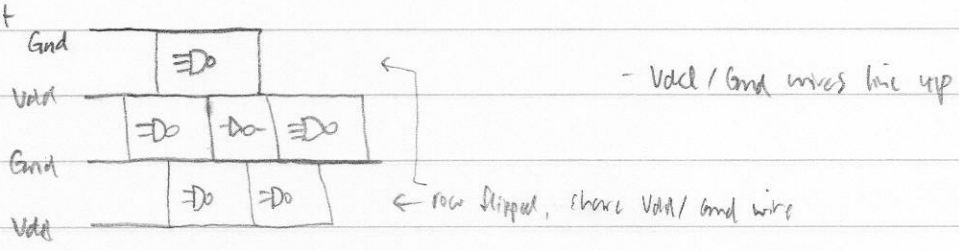
+ signals can easily go under power/ground



• Use wider wires (6λ for link 5), large (many) contacts

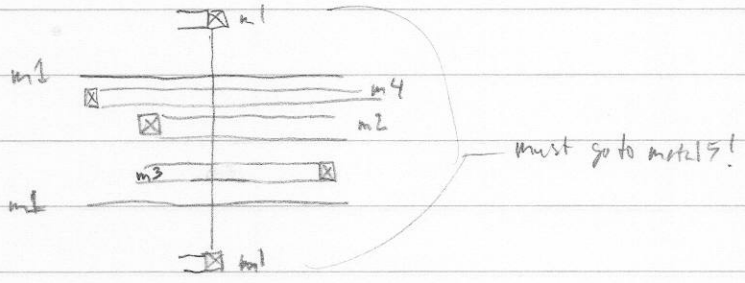
⑤ <see p. 2.1>

⑥ Cell placement



⑦ Metal routing discipline

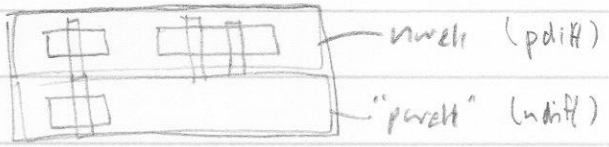
Suppose we want to route across this cell vertically



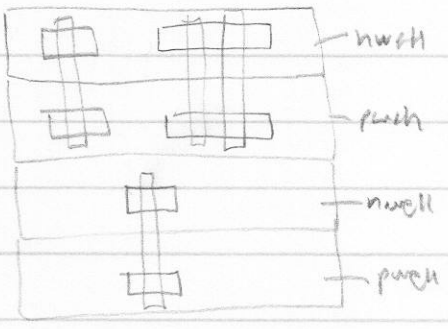
Key point: every wire blocks perpendicular wires from using that layer

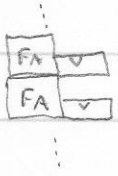
⑤ Rows of diffusion in a cell

* Two:
  - preferable



Four:
- often has large empty spaces
+ easier for more complex cells
- harder to use with std.-height cells
- generally avoid if possible

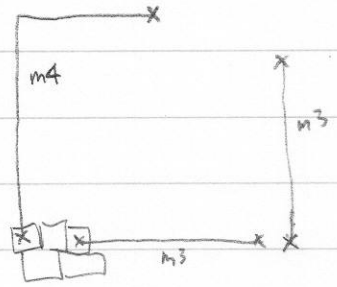




a) Guideline: Try to use only m1 and m2 in small cells

b) Guideline: Use only one direction for each layer.

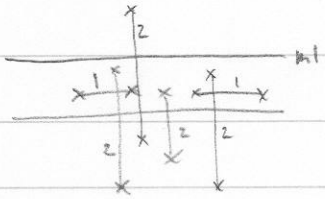
Ex: (bad)



c) Guideline: Alternate directions for each layer

Ex: horizontal: m1, m3, m5

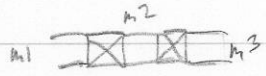
vertical: m2, m4, m6



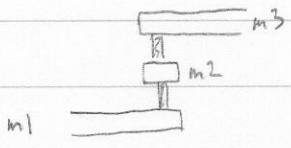
(B) Stack vias: to reduce area

In old days, this was not possible

Ex: m1 to m3



Now thanks to CMP, they can be stacked



Remember m2 is blocked!

Most advanced processes can stack arbitrarily high

but in Magic: pm12c → pdm12c (pdiff, m1, m2)

ndm12c (ndiff, m1, m2)

m123c

m234c

m345c

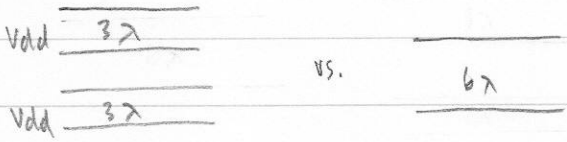
m456c

B. Bacas

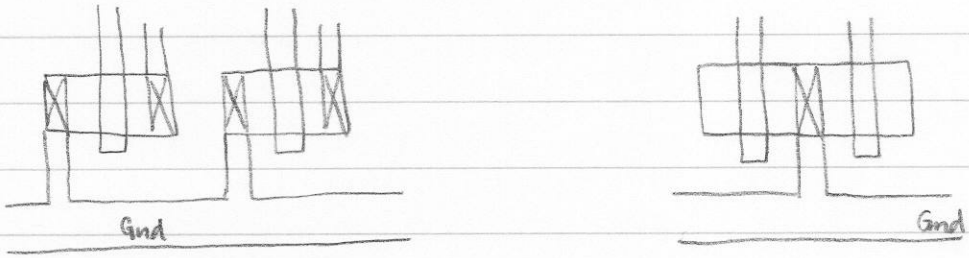
(9) Reduce area

a) share, overlap (Ex: Vdd and Gnd)

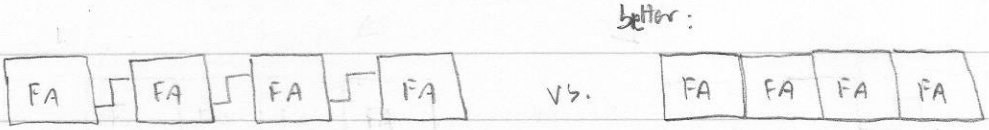
Ex: parallel wires



Ex: 2 inverters

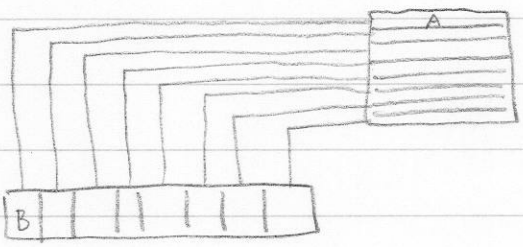


b) Abut

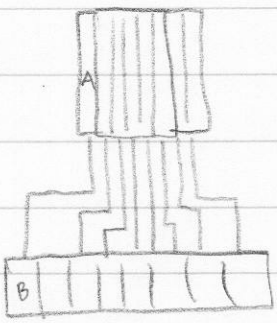


c) Avoid wires that turn corners, if possible

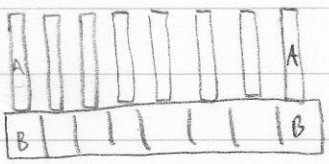
i)



ii)



* iii)



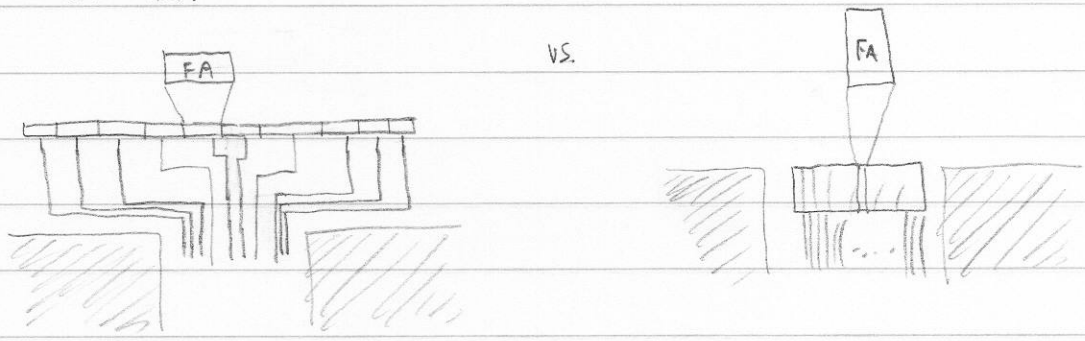
"pitch matching"

pitch of A cells matched with pitch of B cells

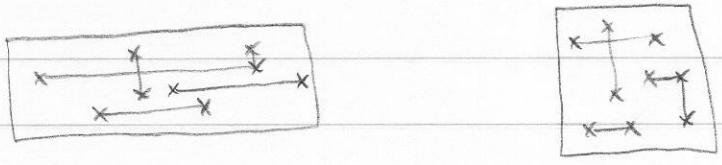
B. Baas

d) Consider shape of overall structure

Ex: 32-bit adder

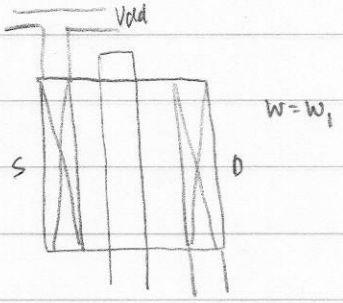


- For an arbitrary block, a square shape will give the shortest total wire length



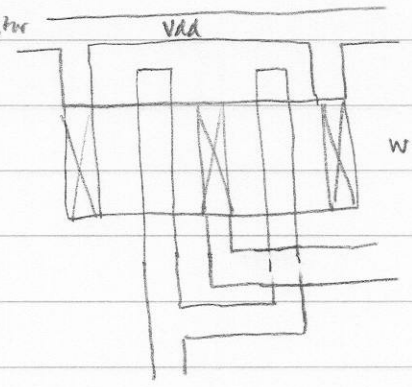
e) Transistor folding (for large devices)

Ex:



- large source & drain caps.
- with very wide trans., will not fit inside the allotted cell height

* fold transistor



- source cap is larger (good)
- drain cap is reduced (good)

(10) Reduce max. delay

$t_p = 0.69 \; R_{MOS} \; C_L$

- Reduce R_{MOS}
  - In layout, means wider transistors
    but this increases load cap. for driving gate
    helps a lot for under-driven nets, diminishing returns eventually

- Reduce C_L

- shorter wires ↔ smaller area ⟶ lower C_L → reduce MOS widths → smaller area ...

- use higher-level metals if possible

(11) Reduce power

$P = C_L V^2 f$

* Reduce C_L

Vdd and f generally set by other requirements

Other more complex techniques possible