Ex: AND

\[
\begin{array}{cccc}
A & B & + & \overline{B} \\
\hline
0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
1 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

+ Only 2 transistors (or 4)
- Non-inverting logic

Ex: XOR

\[
\begin{array}{cccc}
A & B & \overline{B} & \overline{A} \\
\hline
0 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 \\
\end{array}
\]

Ex: XNOR

\[
\begin{array}{cccc}
A & B & \overline{B} & \overline{A} \\
\hline
0 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 \\
\end{array}
\]
Ex: 2-input MUX

A
B
\text{out}
\rightarrow
S
\overline{S}

Ex: 4-input MUX

A
B
C
D
\overline{S_1}
\overline{S_0}
\overline{S_1}
\overline{S_0}
\text{out}

NMOS pull "up" to Vdd poorly

Vdd - V_t
0
0

\overline{Vdd}
IV b) Transmission Gate Logic

Need occasional buffers

Schematic

Layout
Pass Gate Logic

- Can be very small and fast
- May need inverted versions of inputs
- Degraded output levels

Trans. Gate Logic

- Full-swing outputs
- Larger area, cap.

<table>
<thead>
<tr>
<th></th>
<th>Static</th>
<th>Simple Ratiod</th>
<th>Simple Dynamic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Only PUN on</td>
<td>out = 1</td>
<td>out = 1</td>
<td>P-charging</td>
</tr>
<tr>
<td>Only PDN on</td>
<td>out = 0</td>
<td>never</td>
<td>En-1, out = 0</td>
</tr>
<tr>
<td>Both</td>
<td>never</td>
<td>out = 0</td>
<td>never</td>
</tr>
<tr>
<td>Neither</td>
<td>never</td>
<td>never</td>
<td>En-1, out = 1</td>
</tr>
</tbody>
</table>
Ch. 4 - Wires

Chip consists of:

1) Transistors for "work"

→ 2) Interconnections between transistors ("wires")
   a) Signals
   b) Power + Ground

3) Misc.
   - I/O pads

Signals can be routed in:

- Diffusion only short distances \( \approx 5-10 \mu \text{m} \)
- Poly " " " 100 \( \mu \text{m} \)
- Metal most cases

Power/Ground

Always metal

Capacitance

A) Bottom plate or parallel plate

Assume \( \vec{E} \) normal to substrate and wire
\[ C_{wire} = \varepsilon \frac{W L}{t} \]

\( \varepsilon = \text{permittivity of dielectric} \)

\( \varepsilon = \varepsilon_r \varepsilon_0 \quad \varepsilon_0 = 8.85 \times 10^{-12} \text{ F/m} \)

\( \varepsilon_r = 1 \quad \text{free space} \)

\( \varepsilon_r = 3.9 \quad \text{SiO}_2 \)

B) Fringing

C) Estimate of Bottom Plate + Fringing

\[ C_{pp} + C_{fringe} = \varepsilon \frac{W - W/2}{t} + \frac{2\pi t}{\log \left(t/4\right)} \]

Fringing more important for narrower wires
Traditional wire model

\[ R = 0 \]

All cap. to substrate

\[ L = 0 \]

Older technologies

- Slow rise + fall \[ \rightarrow L \text{ dil/ats low} \rightarrow \text{ignore } L \]
- \( t_p \) long
  - gate delay \( \gg \) wire delay \[ \rightarrow \text{ignore } R \]
- Wider and flatter aspect ratios
- Faster metal layers
  - 60nm CMOS \[ \rightarrow \text{2 metal layers} \]

\[ \begin{array}{c}
1 \mu\text{m}^2 \\
2 \mu\text{m}^2 \\
3 \mu\text{m}^2 \\
7 \mu\text{m}^2 \\
11 \mu\text{m}^2
\end{array} \]

Newer technologies

- Wires are thinner with tall aspect ratios
- Many metal layers: 32nm \[ \rightarrow \text{N metal layers} \]
- Resistance increasing
- Intralayer cap significant
- Fast \( t_r \) and \( t_{fall} \) \[ \rightarrow \text{consider } L \]
### Table

<table>
<thead>
<tr>
<th>Condition</th>
<th>Fringe</th>
<th>Fringe + Plaque</th>
<th>Poly - Field</th>
<th>M1 - Field</th>
<th>M5 - Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 aF/μm²</td>
<td>22 aF/0.125 μm² wide/μm²</td>
<td>30 aF/μm²</td>
<td>5.2 aF/μm²</td>
<td>2.6 aF/0.15 μm² wide/μm²</td>
<td></td>
</tr>
<tr>
<td>81 aF/μm²</td>
<td>54 aF/μm²</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.1 aF/0.125 μm² wide/μm²</td>
<td>91</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.1 aF/0.125 μm² wide/μm²</td>
<td>1.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Diagram

![Diagram](image)

### Notes

- For the board, resistance and L for fly back
- 13V 50 Watt → 38 amps
- Power: 5V 5 ma / 1 amp
- Ev: 0.25 Vm

---

*Note: The image contains handwritten notes and a diagram.*