speed up wires:

\[ t_p = k v c L^2 \]

1) make wire shorter - layout
2) possibly increase width of wire
   - e.g., resistive materials like poly
3) possibly use a layer with lower R, lower C
   - e.g., higher level metal
4) pipeline circuit
   - architectural changes too.
5) Insert repeater along wire
   Ex: wire length L

\[ \text{delay} = k v c L^2 \]

\[ \begin{align*}
\text{delay} &= k v c \left( \frac{L}{3} \right)^2 \quad \text{(b)}
\end{align*} \]

\[ \text{delay} = \frac{k v c L^2}{3} + 2 \text{Inr Delays} \]
Rules of Thumb

RC delays should be considered when:

1) \( t_{\text{wire}} \gg t_{\text{gate}} \)

\[
\text{critical length of wire} = L_{\text{crit}} = \sqrt{t_{\text{gate}}/0.35 \, \text{RC}}
\]

2) rise/fall time is smaller than RC

\( \text{rise or fall} < RC \)

Transmission Lines

Signal velocity = \( v = \frac{1}{\sqrt{LC}} \)

\( L = \text{inductance}/\text{length} \)

Characteristic impedance \( Z_0 = \sqrt{\frac{L}{C}} \)

Typical on-chip \( Z_0 \approx 10 \text{ - } 200 \Omega \)

Best performance requires the wire is terminated

1) Parallel Term.

\[ \text{Driver} \rightarrow Z_0 \rightarrow R = Z_0 \]

2) Series Term

\[ R = Z_0 - Z_d \]

\( Z_d = \text{driver output impedance} \)
3) Thermis

4) AC

---

(1) Breakup $C_{\text{TOTAL}}$ and $R_{\text{TOTAL}}$ into $N$ pieces

$$R = \frac{R_{\text{TOTAL}}}{N}$$

$$C = \frac{C_{\text{TOTAL}}}{N}$$

(2) "T" models:

$$T_1 = \begin{array}{c}
\frac{R_{1/2}}{2} \\
C \\
\frac{R_{1/2}}{2}
\end{array}$$

$$T_2 = \begin{array}{c}
\frac{R_{1/4}}{2} \quad \frac{R_{1/2}}{2} \quad \frac{R_{1/4}}{2} \\
\frac{C_{1/2}}{2} \quad \frac{C_{1/2}}{2}
\end{array}$$

Fig 4.26, p. 171
(3) **π models**

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Memories

I. "Single Bit" memories
   - SR latch
   - FF Flip Flop

II. "Array" memories
   1) Read-Write
      a) 6T SRAM
         - store data
      b) multi-port
         - MR + 2RD
         \[ A = B + C \]

   2) NVRWM: non-volatile rd/wr memory
      - Flash: ROM at typical voltages, erasable at high voltages
      - EPROM: erasable with UV light

   3) ROM
      - Programmed at manufacture time
Differential Bitlines

- Can sense very small voltage differences
- Solid noise robustness

SRAM Cell
b) Multi-port SRAM