Reset-able and Enable-able Registers

- Sometimes it is convenient or necessary to have flip-flops with special inputs like reset and enable.
- When designing flip-flops/registers, it is ok (possibly required) for there to be cases where the always block is entered, but the reg is not assigned.
- No fancy code, just make it work.
- Normally use synchronous reset instead of asynchronous reset (easier to test).
Reset-able and Enable-able Registers

- Example FF with reset and enable (reset has priority)

<table>
<thead>
<tr>
<th>reset</th>
<th>enable</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Do nothing</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>D Flip-Flop</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Reset? or Do nothing?</td>
</tr>
<tr>
<td>1</td>
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<td>Reset, Q=0</td>
</tr>
</tbody>
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always @(posedge clk) begin
  if (reset) // highest priority
    out <= #1 1'b0;
  else if (enable)
    out <= #1 c_out;
  // ok if no assignment (out holds value)
end
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always @(posedge clk) begin
  if (enable) begin  // highest priority
    if (reset)
      out <= #1 1'b0;
    else
      out <= #1 c_out;
  end
  // It is ok if there is no assignment to “out” in some
  // cases (out is not assigned when enable==0 in which
  // case out holds its value). Recall that this is never
  // ok for combinational logic.
end
Reset-able and Enable-able Registers

- Use reset-able FFs only where needed
  - Reset-able FFs are a little larger and higher power
  - Requires the global routing of the high-fanout reset signal

reset only these two registers, but now reset must be enabled for at least 3 clock cycles

\[ \cos(x) \]