Verilog Register Assignments

- Rule #5 (always follow in this class): Use only edge-triggered flip-flops and never transparent (clock level-sensitive) latches
- Edge-triggered flip-flops are generally robust with regards to clocking
- Transparent latches are vulnerable to signals racing through more than one latch during a single clock pulse; solutions are generally non-trivial
  - Requiring a minimum delay between latches works but adds area and power dissipation
  - Requiring a maximum pulse width on clocks (likely << 50%) can be problematic
  - A robust but tedious solution is to use two clocks with different phases and requiring consecutive latches to use clocks of differing phases