Detecting Signal Transitions

• Want to design a state machine/circuit that is sensitive to a change in an input signal (e.g. change from 0 to 1).

• Can be awkward designing a FSM for signal transitions.

• Can’t use signal as a clock – leads to poor timing and unreliable circuits.

• Solution: Make a circuit to indicate a transition in an input signal.
Simple Circuit For Edge Detection

Input Signal → D Q → n → Rising Transition

Clock

Input Signal
n
Rising Transition
Timing if Input Signal arrives late in clock cycle

**Diagram:**
- **Input Signal**
- **D Flip-Flop**
- **n**
- **Rising Transition**

**Waveforms:**
- **Clock**
- **Input Signal (Late Arriving)**
- **n**
- **Rising Transition**

The diagram illustrates how a late arriving input signal affects the timing of a rising transition in a digital circuit.
If needed, Rising Transition can be registered
Circuit operates the same with late arriving inputs
Example Verilog module for edge detection with registered output

module edge_detection(
    input clock,
    input input_signal,
    output rising_transition
);

// declarations
reg n;
reg rising_transition;
wire rising_transition_c;

// logic to detect 0 in previous cycle and 1 in current cycle
assign rising_transition_c = ~n & input_signal;

// flip-flop instantiations
always @(posedge clock) begin
    n <= #1 input_signal;
    rising_transition <= #1 rising_transition_c;
end
endmodule