Tune Example

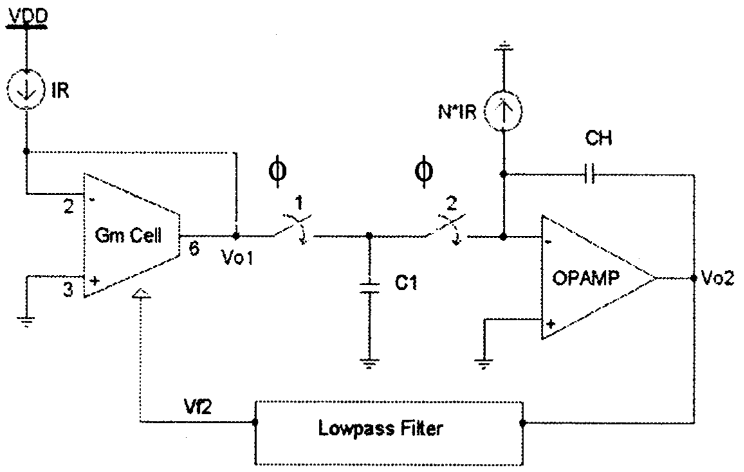

Fig. 4. Simplified Tuning Loop.

The reference tuning loop uses a Gm cell in feedback as shown in simplified form in Fig. 4 [4]. A constant current I_R is pushed into the Gm cell, producing a voltage $V_{o1} = I_R/g_m$. ϕ_1 and ϕ_2 are two non-overlapping clocks with frequency f_{clock}. During ϕ_1, the capacitor C_1 is charged to V_{o1}. During ϕ_2, the charge on C_1 is transferred to capacitor C_H. Also, a constant current NI_R is drawn from C_H. The average value of the opamp output, V_{f2}, is used to tune the transconductance of the Gm cell.

When the loop reaches steady state, the charge injected onto C_H by C_1 during ϕ_2 equals the charge removed from C_H by NI_R in one clock period. Therefore V_{o2} is periodic and V_{f2} is constant. In steady state,

$V_{o1} = \frac{I_R}{G_m}$ (1)

$$Q_{C1} = C_1 V_{o1} = N I_R T \,, = Q_{IR} \qquad (2)$$

where $T = 1/f_{clock}$ is the clock period. Substituting $V_{o1} = I_R/g_m$ into (2) and simplifying gives

$$\frac{C_1}{g_m} = NT = \frac{N}{f_{clock}} \,, \qquad (3) \Leftarrow (1)+(2)$$

where g_m is the transconductance of the Gm cell. Hence, C_1/g_m depends on the clock frequency f_{clock}, which is derived from a crystal oscillator, and N, the ratio of DC currents that can be accurately defined in a CMOS process.

A more detailed block diagram of the tuning loop is shown in Fig. 5. The clock frequency is 6.25MHz and the DC current ratio N is 0.2. Using these values in (3), C_I / g_m = 32ns. If C_I has the same nominal value as C_f (=0.6pF) in the AC coupler, then g_m = 18.8μA/V. With $I_R \leq$ 5μA in Fig. 5, the nominal differential output voltage of the Gm cell is $\leq$ 0.53V. To have a large g_m tuning range, the Gm cell should allow an output swing of >1.0V.

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A 10.7-MHz 68-dB SNR CMOS Continuous-Time Filter with On-Chip Automatic Tuning

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