1. The circuit below is a differential Sample-and-Hold circuit. Each NMOS transistor acts as a switch, controlled by the clock PHI.

![Circuit Diagram]

a) Assume that PHI is high (V_{PHI} = 5V) and each NMOS transistor is in the triode region, with V_{DS} = 0V. Find W/L to give an on-resistance R_{on} of 40 k\Omega for each transistor. Assume the two inputs are both 0 V for this calculation.

\[
W/L = \frac{1}{k_n \frac{w}{L} (V_{GS} - V_T)}
\]

\[
= \frac{1}{180 \frac{A^2}{V^2} \left( \frac{w}{L} \right) (5V - 1V)} = 40 \text{k}\Omega
\]

\[
\Rightarrow \frac{w}{L} = 0.035
\]
b) It is important that the capacitors and transistors are closely matched. You are allowed 200 (\(\mu m\))^2 of total area for the top plates of the two capacitors. Sketch the layout of the top plates for the two capacitors. Give the dimensions of the capacitors on your drawing. (For this part, the most important thing is capacitor matching. Don't worry about the -3 dB frequency of the filter or the capacitor values.)

Use max area, close together,

\[
\begin{array}{c}
L \\
\hline
\end{array}
\]

\[
\begin{array}{c}
L \\
\hline
\end{array}
\]

(could include common centroid)
2. A two-stage op amp is shown below. It was designed to have a bias current \( IB = 20 \mu A \). However, due to a layout error, the op amp is operating with a bias current \( IB = 10 \mu A \), which is half of the design value. For each parameter below, relate the value of the parameter when \( IB = 10 \mu A \) to the value of the parameter when \( IB = 20 \mu A \). (That is, find the scale factor that relates the two values.)

Assume DC biasing places all the transistors in the saturation region for both values of \( IB \), and further assume that all capacitances do not change when the bias current changes.

![Circuit Diagram]

\[ \frac{R_e}{R} \] values are next to transistors.

ideal voltage buffer.

a) How does the low-frequency voltage gain, \( a_v = \frac{V_{out}}{V_{id}} \), change?

\[ a_v(IB = 10 \mu A) = \frac{V_{out}}{V_{id}} = \frac{1}{2} \cdot a_v(IB = 20 \mu A) \]

\[ a_v = \frac{g_m R_o}{\alpha \sqrt{I_b} \cdot \frac{1}{I_b} \cdot \sqrt{I_b} \cdot \frac{1}{I_b}} = \frac{1}{I_b} \]
b) slew rate \((IB = 10 \, \mu A) = \frac{1}{2} \cdot \text{slew rate} \,(IB = 20 \, \mu A)\)

c) The output resistance of the op amp is \(R_{out}\).
\[R_{out} = \frac{r_{x} \cdot r_{s}}{r_{x} + r_{s}} \propto \frac{1}{I_B}\]

\[\propto \frac{1}{I_B} \propto \frac{1}{I_B}\]

d) dominant pole: \(p_1(IB = 10 \, \mu A) = \frac{0.35}{11} \cdot p_1(IB = 20 \, \mu A)\)
\[p_1 = \frac{-1}{g_m R_0, R_d C_c}\]
\[\alpha = \frac{-1}{\sqrt{C} \cdot \frac{1}{I_B} \frac{1}{I_B}} = - \frac{3}{8}\]
e) The non-dominant pole is $p_2$:

$$p_2(\text{IB} = 10 \ \mu A) = 0.71 \cdot p_2(\text{IB} = 20 \ \mu A)$$

$$p_2 \approx -\frac{g_m}{C_L} \alpha - \sqrt{I_B}$$

\[2\]

f) The upper limit of the op-amp output voltage swing is $\hat{V}_{out}^+$:

Circle one:

$\hat{V}_{out}^+$ (IB = 10 \ \mu A) is LESS THAN, GREATER THAN, SAME AS $\hat{V}_{out}^+$ (IB = 20 \ \mu A)

$$\hat{V}_{out}^+ = 5V - \left| V_{p,\text{SAT}}(mX) \right|$$

$$= 5V - \sqrt{\frac{2I_D(mX)}{k_p(10)}}$$

$I_B \uparrow \Rightarrow \Rightarrow \hat{V}_{out}^+ \downarrow
3. A fully differential op amp with common-mode feedback is shown. Assume all transistors are saturated, and assume $M_1 = M_2 = M_3 = M_4 = M_5$. All transistors have $W/L = 50$. Ignore all capacitances except $C_L$.

![Diagram of the op amp circuit]

a) What is the DC drain current in $M_5$? $I_{D(M5)} = \frac{120 \mu A}{11}$

$220 \mu A - 100 \mu A$
b) What is the differential-mode gain? \( \frac{v_{od}}{v_{id}} = \frac{1}{2} \)

\[
\frac{v_{od}}{v_{id}} \approx g_m \left( \frac{v_{o3}}{g_{m3}v_{o1}} \right) = \left( \frac{1410 \mu A}{0.02 \times 10 \mu A} \right) \left( \frac{425 \mu A}{0.02 \times 110 \mu A} \right) = 1.36 M
\]

c) What is the slew rate? \( \frac{dV_{od}}{dt} = \frac{44 \text{ V}}{\mu \text{sec}} = 44 \times 10^6 \text{ V/sec} \)

\[\text{max } I_{out} = 110 \mu \text{A} \]

flows thru two 5 pF caps in series

\[\Rightarrow \frac{dV_{od}}{dt} = \frac{I}{C} = \frac{110 \mu \text{A}}{2.5 \text{ pF}} = 44 \text{ V/\mu sec} \]
A fully differential op amp with common-mode feedback is shown. Assume all transistors are saturated, and assume $M1 = M2 = M3 = M4 = M5$. All transistors have $W/L = 50$. Ignore all capacitances except $C_L$.

a) What is the DC drain current in $M5$? $I_{D(M5)} = \frac{120 \mu A}{220 \mu A} - 100 \mu A$
4. Use Blackman's impedance formula to compute the output resistance of the circuit below. Compute the return ratios with respect to the $g_m$ controlled source of M1. Assume the transistor is saturated. Give the results in terms of $R_L$ and transistor parameters that could be computed, such as $g_m$, $r_o$, etc. Ignore all capacitances in this problem.

\[ V_{DD} \]

\[ V_{in} \quad - \quad + \quad V_{out} \quad - \quad R_L \quad \leftarrow \quad R_{out} \]

a) What is $R_{out}$ when $g_m(M1) = 0$? $R_L \parallel r_o$

\[ R_L \parallel r_o \]

b) What is $RR(g_m(M1)$ with output port open)? $g_m \left( r_o \parallel R_L \right)$

\[ i_t(r_o \parallel R_L) = -N_x \]

\[ R_L \]

\[ RR = - \frac{i_r}{i_t} = g_m \left( r_o \parallel R_L \right) \]
c) What is $RR(g_m(M1)$ with output port shorted)?

\[
\text{Short out} \rightarrow N_{out} = N_x = 0 \\
\rightarrow \text{no return current}
\]

d) Now applying Blackman's formula, what is $R_{out}$ of this feedback circuit?

\[
R_{out} = R_{01} R_e \cdot \frac{1}{1 + g_m (R_{01} R_e)}
\]

\[
\left( \approx \frac{1}{g_m} \quad \text{if} \quad g_m (R_{01} R_e) \gg 1 \right)
\]
5. A circuit with a 'floating' NMOS switch and a capacitor is shown below. Assume the capacitor is charged to \( V_x = 6\text{V} \) and the CK signal at the gate is initially 5\text{V} and then falls from 5\text{V} to 0\text{V}. What is \( V_x \) after CK falls to 0\text{V}?

Assumptions:

a) Ignore junction capacitances associated with the transistor.

b) \( \alpha = 0.5 \) (\( \alpha \) = fraction of channel charge that dumps onto the drain node).

c) Gate-to-Drain overlap capacitance: \( C_{OL(GD)} = 0.02 \text{ pF} \).

d) Gate-to-Source overlap capacitance: \( C_{OL(GS)} = 0.02 \text{ pF} \).

\[
\frac{W}{L} = \frac{5 \mu m}{2 \mu m} = 2.5
\]

\[
V_x = 6 \text{V} \quad \text{and} \quad V_{\text{CK}} = 5\text{V} \Rightarrow \text{transistor cutoff. No channel, only } C_{OL} \text{ caps affect } V_x
\]

\( \Delta V_x \) due to the two \( C_{OL} \)'s:

\[
\Delta V_x = \frac{2C_{OL}}{2C_{OL} + 2pF} \left( 0 - 5\text{V} \right) = -9.8\text{mV}
\]

\[
V_x \rightarrow 6\text{V} - 9.8\text{mV} = 5.902\text{V}
\]