1

For the sample-and-hold circuit in Figure 1 estimate the $\frac{W}{L}$ value needed to give $R_{ON} \cdot C_H \leq 0.5 \mu\text{sec}$ for $V_{CK} = 5\text{V}$ and $V_{in} \leq 3\text{V}$. Assume $k' = 60\mu\text{A/V}^2$ and $V_{T(MAX)} = 0.7\text{V}$ (including body effect).

![Sample-and-Hold Circuit for Problem 1](image)

2

A fully differential op-amp with CMFB is shown in Figure 2. All bodies of PMOS transistors are connected to $V_{DD}$, and all bodies of NMOS transistors are connected to $V_{SS}$. Let $X_d = 0$, and use the transistor sizes listed on the table below as well as the transistor data in the SPICE models (see next page).

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W ($\mu\text{m}$)</th>
<th>L ($\mu\text{m}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{1-2}$, $M_{12C}$</td>
<td>64</td>
<td>0.8</td>
</tr>
<tr>
<td>$M_{4-4}$, $M_{26-27}$, $M_{11}$</td>
<td>96</td>
<td>1.4</td>
</tr>
<tr>
<td>$M_{21-24}$</td>
<td>6</td>
<td>0.8</td>
</tr>
<tr>
<td>$M_{14}$, $M_{25}$, $M_{52}$</td>
<td>16</td>
<td>0.8</td>
</tr>
<tr>
<td>$M_{13}$</td>
<td>1.4</td>
<td>0.8</td>
</tr>
</tbody>
</table>

(a) Choose $W$ values for $M_{12}$ and $M_{51}$ so that $|I_{D13}| = 20\mu\text{A}$. Use $L=0.8\mu\text{m}$ for $M_{51}$ and $L=1.4\mu\text{m}$ for $M_{12}$.

(b) Use SPICE to find the low-frequency op-amp gain $v_{od}/v_{id}$, $v_{oc}/v_{ic}$, $v_{od}/v_{sc}$, and $v_{oc}/v_{sc}$ with the CMFB active. **NOTE:** To get HSPICE to compute the differential output voltage correctly using 'v(out1,out2)', you must include '.options acout=0' in your HSPICE input file. For the op-amp inputs, use $V_{IN(CM)} = -0.65\text{V}$.

(c) Calculate the output slew rate $dV_{od}/dt$ if a 4 pF capacitor is connected from each op-amp output to ground.

(d) What is the differential output voltage swing of this op-amp? Assume that $V_{IN(CM)} = -0.65\text{V}$. (Ignore the body effect.)
(e)** Repeat (b) when the input transistors are mismatched with \( W_1 = 63\mu m \) and \( W_2 = 65\mu m \).

(f)** Repeat (b) when the load transistors are mismatched with \( W_3 = 95\mu m \) and \( W_4 = 97\mu m \).

**Note: \( V_{OS} \neq 0 \) with mismatched transistors.

(g) It is possible to bias the op-amp without \( M_{51} \). What change in device \( W/L \) should be made to \( M_{52} \) to keep the op-amp unchanged when \( M_{51} \) is deleted?

(h) Can you see any advantage to making the change described in (g)?
During one clock phase in a SC filter, the op-amp in problem 2 is in the configuration shown in Figure 3.

(a) Apply a 1-V step as a differential input, using SPICE. What is the slew plus settle time to within 0.5% of the final value?

(b) What is the slew rate? How does this compare with the calculation of $\frac{I_{\text{bias}}}{C}$?

Note: You'll have to add DC feedback to this circuit; this feedback should not affect the circuit above about 10kHz. One way to do this is to put a very large resistor across each 1.5 pF cap: [e.g., rfb x y 1.0t].

SPICE MODELS: 0.4 µm CMOS

```
.MOSN NMOS LEVEL=3
+ TOX=0.8000E-08 XJ=0.150000U TPG=1 PHI=0.600000 DELTA=2.1370E-01 + LD=9.0003E-08 VTO=0.60 GAMMA=0.5947 UO=450 THETA=1.9240E-01 + RSH=1.7260E+01 KP=1.96E-04 NSUB=1.2706E+17 NFS=6.0410E+11 + VMAX=1.8610E+05 ETA=2.1370E-02 KAPPA=8.4220E-02 CGDO=3.5E-10 + CGSO=3.5E-10 CGBO=3.0251E-10 CJ=5.2E-04 MJ=0.59 CJSW=1.2E-10 + MJSW=0.31 PB=0.98 ACM=3 HDF=0.4u

.MOSP PMOS LEVEL=3
+ TOX=0.8000E-08 XJ=-0.150000U TPG=-1 PHI=-0.80 GAMMA=0.5200 UO=-137.3 THETA=1.6710E-01 + LD=9.0000E-08 VTO=-0.80 GAMMA=0.5200 UO=137.3 THETA=1.6710E-01 + VMAX=3.0560E+05 ETA=-1.8760E-02 KAPPA=5.9230E+00 CGDO=3.5E-10 + CGSO=3.5E-10 CGBO=3.0251E-10 CJ=9.1191E-04 MJ=0.49 CJSW=1.2E-10 + MJSW=0.201 PB=0.96 ACM=3 HDF=0.4u
```

You can copy the SPICE MODELS file from: `/home/hurst/212/MOS_models_0.4um`