Tinoosh (Tina) Mohsenin

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RESEARCH INTERESTS

High performance and energy-efficient computation, including algorithm enhancements, application mapping/software development on many-core architectures, and VLSI design of ASICs and reconfigurable architectures that support networking and communications, signal processing, error correction, and biomedical applications.

Single-chip solutions targeted for low-power embedded systems through a co-design of programmable cores and application-specific processors.

EDUCATION

University of California, Davis — Expected June 2010
Ph.D. in Electrical and Computer Engineering
Adviser: Prof. Bevan Baas

Rice University — September 2003
M.S. in Computer Engineering
Adviser: Prof. Scott Rixner

Sharif University of Technology, Iran — September 1999
B.S. in Control Systems

PUBLICATIONS

Tinoosh Mohsenin and Bevan Baas, "A Split-Decoding Message Passing Algorithm for Low Density Parity Check Codes," Accepted for publication in Journal of VLSI Signal Processing.

Tinoosh Mohsenin and Bevan Baas, "Trends and Challenges in LDPC Hardware Decoders," Asilomar Conference on Signals, Systems and Computers (ACSSC), November 2009, **Invited**.

Tinoosh Mohsenin and Bevan Baas, "High Throughput and Energy Efficient LDPC Decoders using Multi-Split-Row Threshold Method," SRC TECHCON, September 2009.

Tinoosh Mohsenin, Dean Truong and Bevan Baas, "An Improved Split-Row Thresholding Decoding Algorithm for LDPC Codes," IEEE International Conference on Communications (ICC'09), June 2009.

Tinoosh Mohsenin, Dean Truong, and Bevan Baas, "Multi-Split-Row Threshold Decoding Implementations for LDPC Codes," IEEE International Symposium on Circuits and systems (ISCAS '09), May 2009.

Tinoosh Mohsenin, Pascal Urard and Bevan Baas, "A Thresholding Algorithm for Improved Split-Row Decoding of LDPC Codes," Asilomar Conference on Signals, Systems and Computers (ACSSC'08), October 2008.

Dean N. Truong, Wayne H. Cheng, **Tinoosh Mohsenin**, Zhiyi Yu, Anthony T. Jacobson, Gouri Landge, Michael J. Meeuwsen, Christine Watnik, Anh T. Tran, Zhibin Xiao, Eric W. Work, Paul V. Mejia, Bevan M. Baas, "A 167-Processor Computational Platform in 65 nm CMOS," IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 4, pp. 1130-1144, April 2009, **Invited**.

Dean Truong, Wayne Cheng, **Tinoosh Mohsenin**, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor Computational Array for Highly-Efficient DSP and Embedded Application Processing," In Proceedings of the IEEE HotChips Symposium of High-Performance Chips, (HotChips 2008), August 2008.

Dean Truong, Wayne Cheng, **Tinoosh Mohsenin**, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling," Symposium on VLSI Circuits, pp. 22-23, June 2008.

Tinoosh Mohsenin, Bevan M. Baas, "High-throughput LDPC Decoders Using A Multiple Split-Row Method," In Proceedings of the 32nd International Conference on Acoustics, Speech, and Signal Processing (ICASSP'07), vol.2, pp. II-13-16, April 2007.

Tinoosh Mohsenin, Bevan M. Baas, "Split-Row: A Reduced Complexity, High Throughput LDPC Decoder Architecture," In Proceedings of the IEEE International Conference of Computer Design (ICCD '06), pp. 320-325, October 2006.

Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Dean Truong, **Tinoosh Mohsenin**, Bevan Baas, "AsAP: An Asynchronous Array of Simple Processors," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 3, pp. 695-705, March 2008.

Ryan Apperson, Zhiyi Yu, Michael Meeuwsen, **Tinoosh Mohsenin**, Bevan Baas, "A Scalable Dual-Clock FIFO for Data Transfers between Arbitrary and Haltable Clock Domains," IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol. 15, no. 10, pp. 1125-1134, October 2007.

Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, **Tinoosh Mohsenin**, Dean Truong, Jason Cheung, "AsAP: A Fine-grain Multi-core Platform for DSP Applications," IEEE Micro, vol. 27, no. 2, March/April 2007, **Invited.**

Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Daniel Gurman, Chi Chen, Jason Cheung, Dean Truong, **Tinoosh Mohsenin**, "Hardware and Applications of AsAP: An Asynchronous Array of Simple Processors," In Proceedings of the IEEE HotChips Symposium on High-Performance Chips (HotChips 2006), August 2006.

Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, **Tinoosh Mohsenin**, Mandeep Singh, Bevan M. Baas, "An Asynchronous Array of Simple Processors for DSP Applications," In Proceedings of the IEEE International Solid-State Circuits Conference, (ISSCC '06), pp. 428-429, February 2006.

Patrick Murphy, J. Patrick Frantz, Eric Welsh, Ricky Hardy, **Tinoosh Mohsenin** and Joseph Cavallaro, "VALID: Custom ASIC Verification and FPGA Education Platform," Microelectronic Systems Education Conference, (MSE'03), pp. 64-65, June 2003.

In Review

Tinoosh Mohsenin, Dean Truong and Bevan Baas, "A Low Complexity Message Passing Algorithm for Reduced Routing Congestion in LDPC Decoders", Submitted to IEEE Transactions of Circuits and Systems I, in review, **Invited**.

Grant Proposals

"Efficient Hardware for Complex Communication Processors", Principal Investigator: Bevan Baas, Submitted to National Science Foundation (NSF), wrote two sections of the proposal, December 2009.

Tinoosh Mohsenin, and Bevan Baas, "Ultra Low Power 10GBASE-T LDPC Decoder Research Chip", Submitted to STMicroelectronics, wrote all sections of the proposal, August 2009.

Patent

Tinoosh Mohsenin, Pascal Urard and Bevan Baas, "Improved Split-Row Decoding of LDPC Codes," US patent pending, patent serial number: 12/605,078, filed October 2009.

RESEARCH EXPERIENCE

Research Assistant, Adviser: Prof. Bevan Baas May 2005-present
University of California, Davis, Electrical and Computer Engineering Department

Algorithms and architectures for efficient Low Density Parity Check (LDPC) decoder hardware

Development of the *Split-Row, Multi-Split and Split-Row Threshold* decoding algorithms

Designed the algorithms, which significantly reduce wire interconnect and circuit complexity through reduction in data dependency and inter-processor message passing.

Studied the impact of LDPC code matrix properties (e.g. code length and row weight), and *Split-Row*-type algorithm characteristics such as the level of partitioning, correction factor value, threshold value and fixed-point representation on the error correction performance. Theories were verified using empirical simulations on approximately 300 networked computers.

VLSI design of 10 Gigabit Ethernet LDPC decoder chips

Implemented architectures in 180 nm and 65 nm technology of at least eight LDPC decoder chips compatible with the 10GBASE-T 10 Gigabit Ethernet standard. Applied VLSI techniques to build low power and high throughput processor nodes. Analyzed the benefits of the algorithms on silicon area, clock speed and power with the results of multiple backend script generated synthesis and place-and-routed standard-cell designs.

Resulted in a highly efficient LDPC decoder occupying 4.84 mm^2 with an area utilization of 97%, an average throughput of 92.8 Gbps at 1.3 V and an average power of 62 mW at 0.7 V. Best case comparison showed that my decoder silicon area is 3x smaller, with a 6.8x higher throughput, and 4.2x better energy efficiency among the previously reported implemented decoder chips.

Design of a heterogeneous 167-processor chip in 65 nm

Was a key member in a team of graduate students that designed and taped out a 167 processor, 55 million transistor chip, in less than a year. This was the second version of our **As**ynchronous **A**rray of simple **P**rocessors, or *AsAP*,. The massively-parallel MIMD array demonstrated improved efficiency for embedded applications with features such as a globally asynchronous locally synchronous (GALS) architecture and per-processor dynamic voltage and frequency scaling (DVFS) capabilities. At 1.3 V, each programmable processor operates up to 1.2 GHz at 60 mW for a total of 200 GOps/sec per chip.

Responsible for chip development and chip testing

Co-developed parallelized applications to test the chip functionality and performance.

Enhanced computational efficiency of the programmable DSP processors by adding specialized instructions and architectural features.

Integrated and verified GALS compatible shared memory blocks and processor placement on the chip layout.

Was in charge of chip level power distribution network design with five VDDs and three grounds. Analyzed power drops and power pad placement. Designed I/O ring and I/O pads and the glue interface between logic and I/O. Performed analysis on high speed packaging and board design issues with respect to digital I/O modality.

Graduate Researcher, Supervisor: Prof. Ben Yoo Dec. 2003-Sept. 2004
University of California, Davis, Electrical and Computer Engineering Department

First 10 Gbps optical CDMA prototype

Worked in a team of post doctorates and graduate students to implement and demonstrate a DARPA funded 10 Gbps optical CDMA transceiver prototype. Responsibilities included RTL coding of an LDPC decoder and encoder, synthesis, verification and implementation of the decoder and encoder on a six Virtex-II Pro FPGA module platform.

Research Assistant, Adviser: Prof. Scott Rixner Sept. 2002-Sept. 2003
Rice University, Electrical and Computer Engineering Department

Design of an FPGA-based reconfigurable Gigabit-Ethernet/PCI network interface card

Designed and implemented the first generation RiceNIC, which is a reconfigurable and programmable Gigabit Ethernet network interface card (NIC) with significant computation and storage resources used for research on future network interface architectures. Implemented the system in Verilog, verified the design on a Virtex-II Pro FPGA prototyping board, and analyzed RiceNIC's performance on an Opteron server using various TCP payloads.

WORK EXPERIENCE

Summer Intern May 2002-Aug. 2002
Nokia Research Center, Irving, TX

Part of a team that designed the near final prototype for the next generation of CDMA system. Responsibilities included: IF interface digital design for frequency switching, AGC design, RTL coding, logic verification and timing simulation, implementation on FPGA and physical system testing on an RF platform.

Digital Design Engineer Oct. 1999-May 2001
Towzin Electric Engineering Inc., Tehran, Iran

Designed and implemented various automated weigh station systems with Intel 8051 microcontrollers. Wrote the memory controller, keyboard and LCD interfaces in Assembly. Designed and built controller platforms using OrCAD PCB Designer.

TEACHING AND MENTORING EXPERIENCE

Teaching Assistant
University of California, Davis

EEC 100: Circuits II Summer 2005
Directed all discussion classes, graded homework, projects and final exam for an undergraduate analog circuit design course

Eng 006: Engineering Problem Solving Spring 2005
Directed all discussion classes, two different sessions per week. Graded homework, projects and final exam for an undergraduate laboratory concentrated on signal processing analysis using Matlab.

Sharif University of Technology, Iran

Digital Systems Design Spring 1999
Directed all discussion classes, designed and graded homework and tests for an undergraduate class on digital logic design.

Guest Lecturer
University of California, Davis

EEC 116: VLSI Design Spring 2009
Prepared notes and delivered a lecture for an undergraduate digital circuit design course.

EEC 272: Embedded System Design Fall 2007
Prepared and delivered LDPC codec programming tutorials for a graduate level course on embedded system architecture and programming.

Student Mentor
University of California, Davis

Graduate Student Mentor Winter 2007-present
Guided first and second year graduate students in the research group for various projects. Responsibilities included development of projects for application programming and software verification of a 167-processor chip during tapeout, and supervised the FPGA implementation of test models for a fabricated chip and lab measurements.

The Society of Women Engineering (SWE) Mentor Winter 2008
Mentored female undergraduate students during their courses in Digital Systems I and Signal and Systems I. Responsibilities included tutoring, homework help and test preparation.

INVITED TALKS

University of Washington, FPGA Seminar
"Algorithms and Architectures for Efficient Low Density Parity Check (LDPC) Decoder Hardware", December 11, 2009.

UC Davis Iranian Women Association, Seminar
"Women in Science and Engineering", November 06, 2009.

Rice University, ECE Seminar
"A 32 Gbps 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder Using Split-Row Threshold Decoding Method ", September 17, 2009.

Texas Instruments, Dallas, TX, Research Seminar
"A 1.6 W 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder", September 16, 2009.

IEEE Santa Clara Valley (SCV) Solid State Circuits Society, Santa Clara, CA, Seminar
"A 32 Gbps 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder Using Split-Row Threshold Decoding Method", August 20, 2009.

Aquantia, Milpitas, CA, Technical Meeting
"A 32 Gbps 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder Using Split-Row Threshold Decoding Method", July 23, 2009.

National Chiao Tung University (NCTU), Taiwan, Research Group Seminar
"Efficient DSP Hardware Implementations", May 15, 2009.

National Taiwan University (NTU), Taiwan, Research Group Meeting
"Efficient DSP Hardware Implementations", May 21, 2009.

Plato Networks, Santa Clara, CA, Technical Meeting
"High Throughput and Low Power LDPC Decoders Using Split-Row Decoding Methods", February 26, 2008.

Jet Propulsion Laboratory (JPL) at the California Institute of Technology, Research Seminar
"High Throughput and Low Power LDPC Decoders Using Split-Row Decoding Methods", March 13, 2008.

CONFERENCE TALKS

Invited Session in Asilomar Conference on Signals, Systems and Computers (ACSSC'09), "Trends and Challenges in LDPC Hardware Decoders", November 2009.

SRC TECHCON 2009, "High Throughput and Energy Efficient LDPC Decoders Using Multi-Split-Row Threshold Method", September 2009.

IEEE International Conference on Communications (ICC'09), "An Improved Split-Row Thresholding Decoding Algorithm for LDPC Codes", June 2009.

IEEE International Symposium on Circuits and Systems (ISCAS'09), "Multi-Split-Row Threshold Decoding Implementations for LDPC Codes", May 2009.

Asilomar Conference on Signals, Systems and Computers (ACSSC'08), "A Thresholding Algorithm for Improved Split-Row Decoding of LDPC Codes", October 2008.

IEEE International Solid-State Circuits Conference (ISSCC) 2008 Student Forum, "An 18 Gbps 2048-bit 10GBASE-T Ethernet LDPC Decoder", February 2008.

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP'07), "High-Throughput LDPC Decoders Using A Multiple Split-Row Method", April 2007.

Annual Industrial Affiliates at UC Davis, " A Multi-core Platform for DSP Applications", Student Poster Presentation, February 2007. Best poster presentation award.

IEEE International Conference of Computer Design (ICCD '06), "Split-row: A Reduced Complexity, High Throughput LDPC Decoder Architecture", October 2006.

Annual Industrial Affiliates at UC Davis, "Hardware Efficient LDPC Decoders", Student Poster Presentation, February 2006.

Industrial Affiliates at Rice University, "Design of an FPGA-based Reconfigurable Gigabit-Ethernet/PCI Network Interface Card", Student Poster Presentation, October 2003.

PROFESSIONAL ACTIVITIES AND MEMBERSHIP

Member of IEEE

Member of IEEE Women in Engineering (WIE)

Member of IEEE Women in Communications Engineering (WICE)

Reviewer of IEEE Journal of Solid-State Circuits (JSSC)

Reviewer of IEEE Transactions on Circuits and Systems-I (TCAS-I)

Reviewer of IEEE Transactions on Signal Processing (TSP)

Reviewer of IEEE International Conference on Communications (ICC)

Reviewer of IEEE International Symposium on Circuits and Systems (ISCAS)

Reviewer of IEEE International Conference on Computer Design (ICCD)

Student volunteer at IEEE GLOBECOME 2006 and SiPS 2008 conferences

AWARDS

Best Poster Presentation Award, Annual Industrial Affiliates, February 2007, University of California, Davis

Graduate Student Travel Award, University of California, Davis, May 2007

Rice University Fellowship, August 2001-May 2002

Ranked 197 among nationwide university entrance examination with more than 1,300,000 participants, August 1994

REFERENCES

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Prof. Behnaam Aazhang
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