UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180A **DIGITAL SYSTEMS I** **Winter 2006**

LAB 5: STATIC HAZARDS, LATCHES AND FLIP-FLOPS

The purpose of this lab is to introduce a phenomenon called *hazards*, which may cause a circuit to malfunction. Also, you will learn about basic memory building blocks (necessary for sequential circuits) by studying several types of latches and flip-flops.

Hardware Required:

4	74LS00 Quad 2-input NAND gate
1	74LS04 Hex INVERTER
1	74LS10 Triple 3-input NAND gate

Preparation

- Read and understand the *entire* lab handout and the relevant sections (Ch. 8.3-8.4 and Ch 11.1-11.5) of the Roth textbook.
- Analyze the function $Y = A * B + B' * C$ using a Karnaugh map. Determine if this function has a static 0-hazard or a static 1-hazard. Using the K-map, derive an equation which implements the same function but eliminates the static hazard.
- For the cross-coupled NAND latch and the clocked S-R latch described in Part B, construct a truth table which shows all inputs at a given time t and the resulting output a short time later ($t+\Delta$, where Δ represents a "short" time period).

Description

Part A. Static Hazards

In the first part of the lab, you will study a special type of hazard, namely *static hazards*. A static hazard is a condition where a single variable change produces a momentary output change where no output change should occur. Static hazards are further classified as either static 1-hazards or static 0-hazards.

Set up the circuit of Figure 1 but connect five inverters in series instead of the one shown in the figure. This is to introduce more delay into the circuit. The circuit is to be an implementation of the function,

$$Y = AB + B'C.$$

This circuit demonstrates the occurrence of a hazard. Due to the delay in the inverter, when B changes from 1 to 0, both inputs of gate 3 may be equal to 1 momentarily. So the output Y becomes 0 for a very short time. To make this delay longer, we add inverters before gate 2.

Observe the output Y on the scope. Connect the B input to your function generator so it will change repeatedly. Increase the frequency of the B input until you can see the hazard. If you cannot see the hazard clearly, connect B to the other scope channel and trigger the scope with that channel. Viewing both channels, you should be able to see the spikes clearly.

Change the number of inverters before gate 2 from five to three.
Q1: Do you see any difference? If so, what is it?

Q2: What would happen if you add more than five inverters of delay into the circuit?
Q3: Why might it not be a good idea to use an even number of inverters of delay?

Redesign the circuit to eliminate the hazard. This can be done by using the method presented in lecture and the textbook. You must determine how to do this and have your design ready before coming to lab. Build the new circuit and check if it still has the hazard.
Q4: What are the other ways to eliminate static hazards?

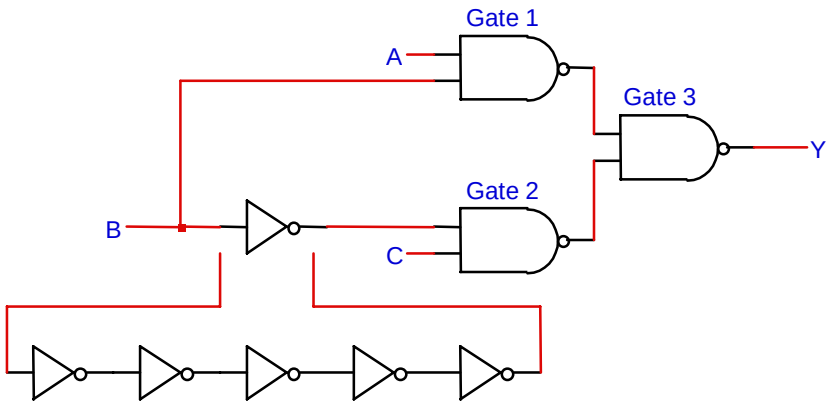

Figure 1

Part B. Flip-Flops

I. Cross-Coupled NAND Latch

a) **Do5:** For the circuit of Figure 2, set up a transition table summarizing the operation of the circuit. This table shows all possible "current" value combinations for *A, B, X,* and *Y* in a truth table, and also shows the resulting "next" values for *X* and *Y*.

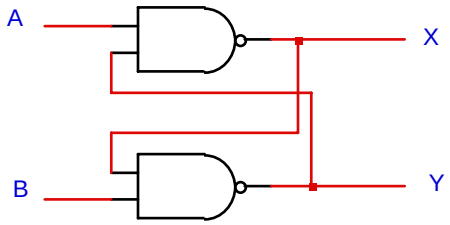

Figure 2

b) Use the circuit to build a bounceless switch as shown in Figure 3. Mechanical switches typically "bounce" when switched—meaning when they transition from open to closed or vice versa, they make several very fast transitions. For example, a switch may transition open -> closed -> open -> closed when it is closed once.
Do6: Explain why the circuit in Figure 3 is bounceless and compare it with a mechanical switch.

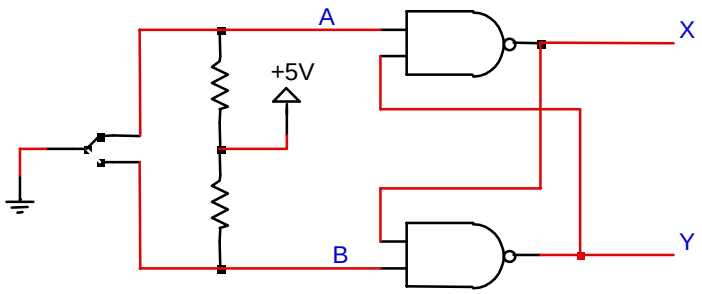

Figure 3

II. Clocked S-R Latch

Set up the circuit shown in Figure 4.

Do7: Make a transition table for the circuit and test it using the bounceless switch as the clock.
Q8: What constraints must be imposed on the inputs S-R?
Q9: In what way does the clock change the performance of the S-R latch?
Q10: How is this useful?
Do11: Determine the longest possible delay from the transition of any input to the transition of any output. State the delay in units of gate delays and give one example input -> internal nodes -> output transition path.

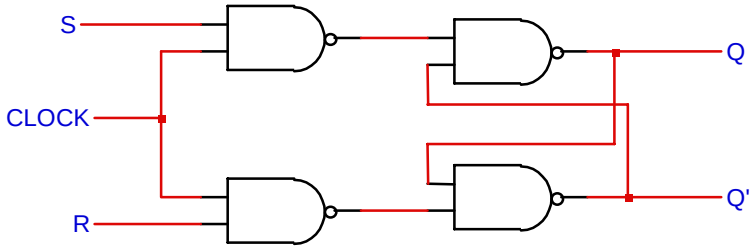

Figure 4

III. Clocked S-R Master-Slave Flip-Flop

Connect two of the clocked S-R latches constructed in Part II in series similarly to what is shown in Figure 11-19 on page 304 of the Roth book. The clock of the second latch (slave) must be the complement of the clock of the first (master) latch.

Test the flip-flop using the bounceless switch as a clock.

Q12: When does the output change values?
Q13: How does it differ from the clocked S-R latch of Part II?
Q14: What is the advantage of this over the clocked S-R latch of Part II?

IV. Positive-Edge-Triggered D Flip-Flop

A very common flop-flop in digital systems is the edge-triggered D flip-flop. Set up the circuit of Figure 5.
Do15: Explain in a few sentences at a high level how the circuit operates and why it is called "edge-triggered."

a) Test the flip-flop using the bounceless switch as a clock.
Q16: When does the output change values?

b) The *minimum setup time* is defined as the time interval during which the data must be stable prior to the active clock transition. The *minimum hold time* is defined as the interval during which a signal must be maintained after the active transition of the clock.
Q17: What is the "active clock transition" for this circuit?

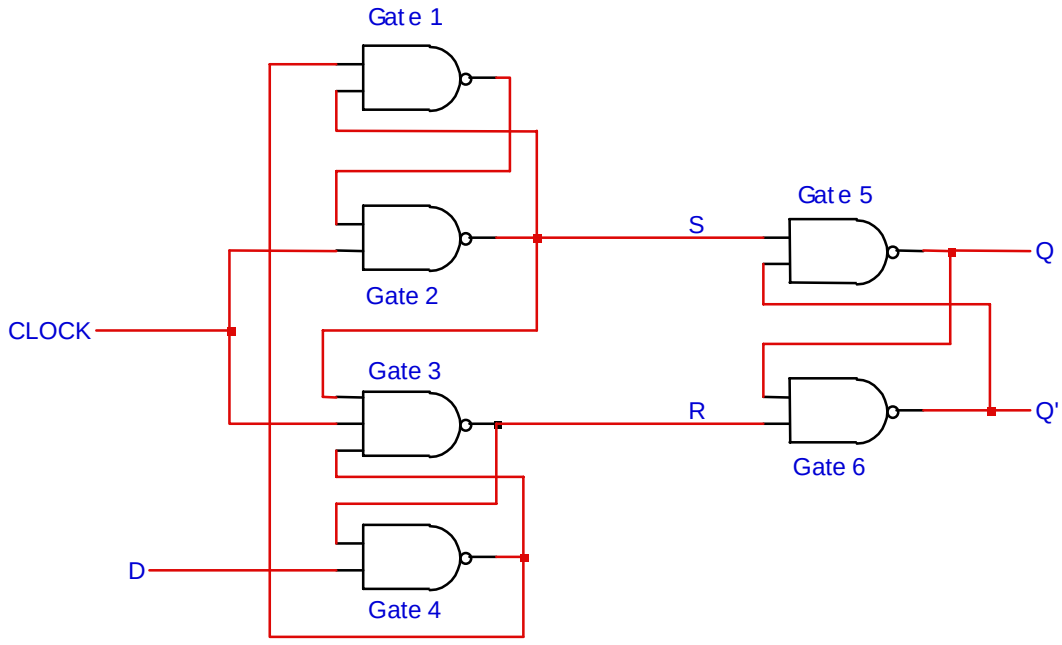

Figure 5: D-type positive-edge-triggered flip-flop

c) Connect a 74LS00 NAND gate as an inverter as shown in Figure 6. Connect the function generator output directly to the *D* input and the inverted clock signal to the *CLOCK* input of your D flip-flop. Measure the set-up time given by this configuration on the scope by displaying the *D* and *CLOCK* inputs on the two channels. The setup time is measured from the point the *D* input signal crosses 2.5 V to the point where the rising clock edge crosses 2.5 V (assuming a 5 V power supply voltage).
Do18: What is your measured setup time?

d) Check the *Q* output with the *D* and *CLOCK* signals generated as shown in Figure 6.
Q19: What output would you expect in the ideal case of zero minimum setup time?
Q20: Which output value do you expect if the minimum setup and/or hold times were violated?
Q21: Which output value did you observe?

e) If you observed a setup time violation in part d, add an additional inverter to the *CLOCK* input to increase the *CLOCK* delay which increases the setup time.
Do22: Check if a setup time violation still occurs.
Do23: Determine how many inverters are required to meet the setup time.

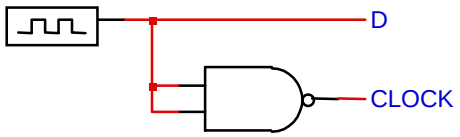

Figure 6: *D* and *CLOCK* inputs for measuring setup time

Lab Report

In your report, answer ALL questions, requested descriptions, and requested explanations in all parts of this handout. Be as complete and precise as possible. In addition, turn in your graded pre-lab and TA verification sheet. (The TA will specify which parts he or she will verify.)

Grading

Prelab	20 points
Lab checkoff	30 points
Hazard shown on scope	(10)
Clocked S-R master-slave latch operation	(10)
D flip-flop operation	(10)
Lab report	50 points
Throughout this document, 23 questions and things to do are numbered in boldface with a label beginning with "**Q**" for questions and "**Do**" for things to be done. Each is worth 2 points.	(46)
Neatness, style, etc.	(4)