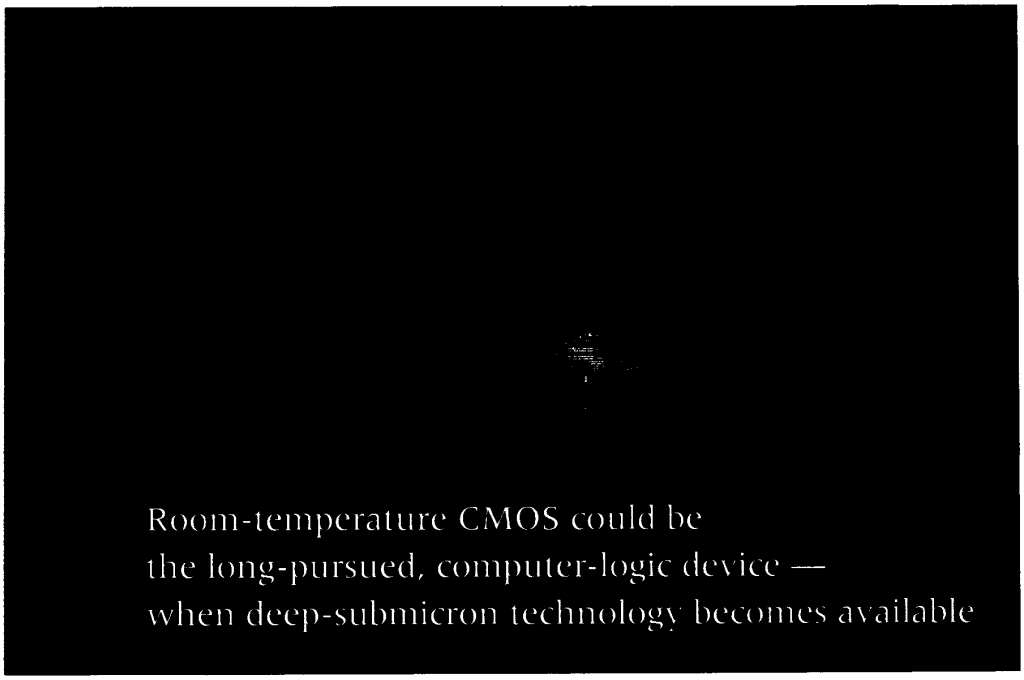
# Deep-Submicron CMOS Warms Up to High-Speed Logic*

by Akira Masaki




*L. Manning/Westlight*

Silicon bipolar devices, particularly those in emitter-coupled logic (ECL), have been accepted as the most useful of the various high-speed technologies since ICs were first introduced into computers. But the possibilities for improving ECL will eventually reach their limits. In anticipation of that time, many alternative technologies have been proposed, including low-temperature CMOS, GaAs, HEMT, and even Josephson junction devices. It is difficult to compare these technologies and predict which technology will be ECL's successor.

Despite the predictive difficulties, it will be indicated in this article that room-temperature CMOS, which heretofore has not been widely recognized as producing very-high-speed devices, can be the

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| Table 1<br>Logic Function Capability (4-bit ALU) | | | |
|---|---|---|---|
| | CMOS (NAND) | ECL | Ratio |
| Total circuit count | 98 | 57 | 1.7 |
| Circuit stages in signal paths (avg.) | 6.1 | 2.9 | 2.1 |

long-pursued post-ECL technology. If it becomes possible to implement high-speed computer logic with room-temperature CMOS, we will no longer need to worry about comparing technologies. Even if equivalent system-performance can be obtained by other technologies, CMOS will win industrial favor because the advanced semiconductor technology established through development of DRAM is directly applicable to CMOS. In addition, the technological compatibility with personal computers, workstations, and small computers benefits all aspects of R&D in high-speed CMOS computers. The ability to scale CMOS down will also allow circuit designs to be inherited through design generations. Last but not least, CMOS's low power dissipation cannot be matched by other technologies, even when applied to high-speed computer logic. As a consequence of the preceding factors, the integration scale achievable with CMOS is the highest of any of the candidate technologies.

### Integrating High-Speed ICs

The scale of integration is often regarded as a non-critical parameter for high-speed computer logic because circuit speed is the primary concern. But integration scale has steadily increased by ten times every five years over the past quarter century (Fig. 1). This rate of increase is the same as that for DRAMs, which is usually stated as four times every three years. This clearly tells us that increases in integration scale have been the source of decreasing cost-performance ratio in computers.

It is not yet known whether this trend will, or should, continue. If it does continue, the gate count per chip will reach two million in the year 2000. Novel high-speed devices will not be able to cope with this complexity in a practical way, and it will not easy for conventional ECL either. Even if individual gate-circuit power is as little as 2 mW, a 2 megagate chip will consume 4 kW — an unmanageably large power.

Fortunately, silicon technology itself should be capable of realizing the required scale of integration since there is no sign that the rate of increase of DRAM-chip integration is slowing. Therefore, in addition to meeting performance requirements, we should make a conscious effort to increase the integration of logic chips.

CMOS can realize the integration but its speed has been insufficient, at least at room temperature. Recently, a fairly fast circuit speed was obtained by decreasing the MOSFETs gate-length to approximately 0.2 μm [1,2]. However, it is not yet clear that very-high-speed computer logic can be made with such CMOS devices. By referring to extensive theoretical developments, we hope to shed some light on this question throughout the remainder of this article [3-9].

### Estimating Logic Performance

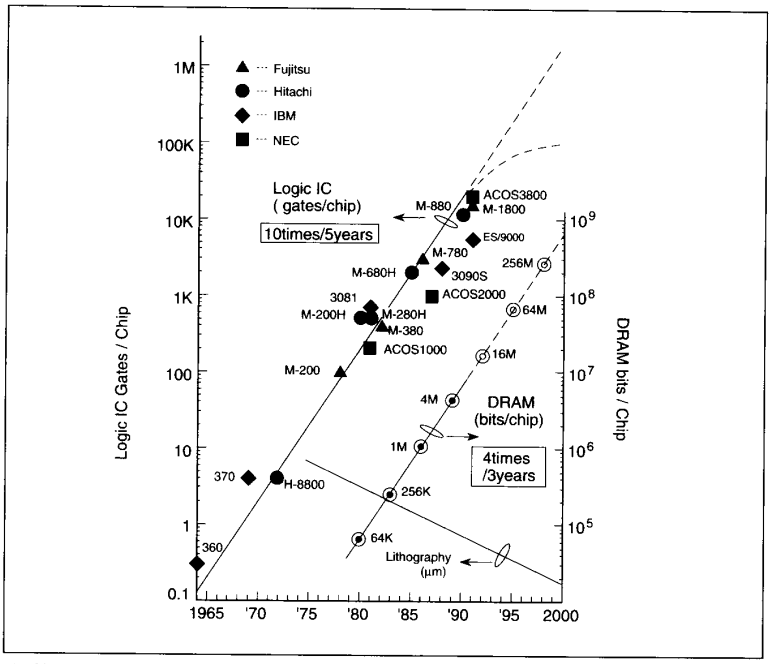
Device performance is usually demonstrated with data from a very lightly loaded ring oscillator, but such data does not directly relate to system performance. While most experts agree when they estimate memory performance, estimating the performance of logic systems has always been much more controversial. Various factors should be considered in such estimates, including the logic-function capabilities of basic circuits, the wire length of logic signal nets, and the power of CMOS circuits in system environments.

*Logic Function Capability*

In assessing the differences in logic-function capabilities among circuits [3,5,6], the essential questions are:

- How many circuits are required in all?
- In each technology, how many circuit stages are required for the critical signal path in a specific functional block?

The real potential of a technology can be grasped only after the second question is fully answered, because it is the power and delay of the functional block, not the unit circuit, that should be minimized. Unfortunately, it is difficult to obtain a general solution to this problem because the results of a design depend strongly upon the logical characteristics of the functional block, as well as upon the differences in the individual abilities of designers. Nonetheless, differences in the logic-func-




*1. Although the integration scale of very-high-speed computer-logic chips is often regarded as non-critical, it has been increasing at the same rate as DRAMs for a quarter of a century.*

tion capabilities of various circuits cannot be neglected.

We can demonstrate the point by comparing the total circuits and the average number of circuit stages in the signal paths of carefully designed 4-bit arithmetic and logical units built with ECL and simple CMOS NAND (Table 1). The circuit count and number of circuit stages required to implement a specific logic function are smaller for ECL. Results obtained in various case studies [5,6] lead us to conclude that simple CMOS NAND requires roughly twice as many total circuits and circuit stages as ECL.

*Wire Length of Logic Signal Nets*

Delays caused by wire capacitance significantly affect circuit performance. Estimating the wire length of logic signal nets is therefore indispensable when evaluating performance in system environments.

A simplified structure for a logic-circuit cell array, which could be an LSI chip, a module substrate, or a printed circuit board, provides a basis for wire-length estimates (Fig. 2). The wire length of the signal net, $L_w$, is $n_{pp}$ x $l_{pp}$ x $p$, where $n_{pp}$ is the number of pin-to-pin (or terminal-to-terminal) wires per signal net, and $l_{pp}$ is the terminal-to-terminal wire length expressed in terms of the average center-to-center spacing of the cells, $p$.

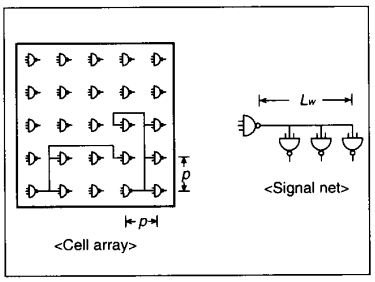
An equation for estimating $l_{pp}$ [10], which is applicable to two-dimensional square arrays, was derived from the Rent's Rule equation [11]. By extending this work, we obtained equations for estimating various types of two- and three-dimensional packaging structures [7]. One of these is extremely useful:

$$l_{pp} = \frac{1 - 2^{2(r-1)}}{6\,(1 - 2^{2(r-1)L})} \cdot \left\{ \frac{7\,(2^{(2r-1)L} - 1)}{2^{2r-1} - 1} - \frac{1 - 2^{(2r-3)L}}{1 - 2^{2r-3}} \right\}$$

where L is the base 2 logarithm of the number of circuit cells in the x and y directions, and $r$ is the exponential coefficient in the Rent's Rule equation.

*Power Consumption of CMOS Circuits*

A CMOS circuit consumes energy only during switching. Estimating its power consumption in a realistic system environment therefore requires us to obtain the circuit's switching frequency in actual systems. To help us analyze the problem, let's introduce a quantity ($k$) that is defined as the average switching period ($T$) of the circuits in a system, divided by the circuit delay in the system ($t_{sd}$) [4,5]. The definition of $k$ is similar to that of the CMOS switching factor defined in [12].




*2. The signal net model for a logic-circuit cell array provides a convenient basis for wire-length estimates.*

The value of $k$ is independent of the hardware technology; it depends solely upon the logical structure of the system as long as the performance potential of the circuit is fully utilized. If sophisticated logic is used, $k$ becomes smaller; that is, switching occurs more frequently.

There are several methods for obtaining the value of $k$ [4,5]:

(1) Investigate the logical structure of the system.

(2) Measure the switching frequency of logic signals in system operation.

(3) Measure power dissipation in systems built with CMOS.

(4) Count the number of times the circuits switch by simulating the logical operation of the system.

Experimental values obtained with methods 2 and 3 are in good agreement with the estimated values from methods 1 and 4 (Table 2). We can therefore conclude that $k$ is within the range of 20 to 200 for most computer systems. We will assume $k$ to be 40.

*Load-driving Capability and Wire Delay*

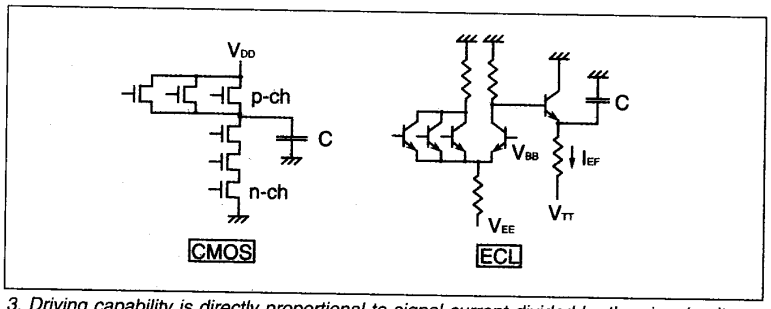
Load-driving capability is one of the most important characteristics of computer-logic

Table 2: K Values (T/tsd)

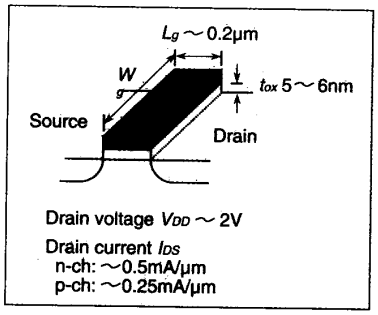
| | Minicomputer | | Large-scale computer |
|---|---|---|---|
| | A | B | |
| (1) Analysis of logic Structure | 180 | 120 | 60 ~ 20 |
| (2) Measurement of switching frequency | 200 | | |
| (3) Measurement of power of CMOS computer | | 170 ~130 | |
| (4) Logic Simulation | | | 80 ~ 30 |

Table 3. Device Parameters for Very-High-Performance CMOS Logic

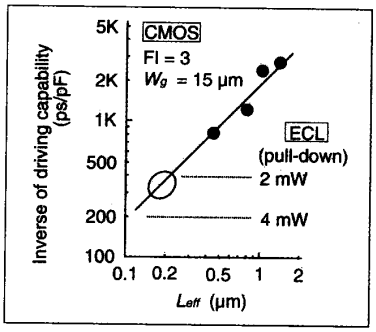
| | Intrablock 3NAND | Interblock buffer |
|---|---|---|
| Drain voltage $V_{DD}$ | 2V | |
| Gate length $L_g$ | 0.2 µm | |
| Gate oxide thickness $t_{ox}$ | 5 ~ 6 nm | |
| Gate width $W_g$ | 15 µm | 75 µm |
| Drain current $I_{DS}$ (n-ch) | 7 mA | 35 mA |
| (p-ch) | 3.5 mA | 18 mA |
| Input capacitance $C_{in}$ | 0.05 pF | 0.25 pF |
| Wire capacitance | 0.2 pF/mm | 0.2 pF/mm |
| Wire Resistance | 100Ω/mm | 6Ω/mm |
| Switching energy (circuit) | 0.5 pJ | 2.5 pJ |
| (load) | 3.0 pJ/pF | 3.0 pJ/pF |
| Driving capability | 400 ps/pF | 60 ps/pF |
| Circuit delay (F0=1, $C_w$=0 pF) | 80 ps | 40 ps |
| (F0=3, $C_w$=0.2 pF) | 200 ps | |




*3. Driving capability is directly proportional to signal current divided by the signal voltage. CMOS's signal voltage is as large as 5 V and its driving current is small; ECL's signal voltage is as small as 0.5 V and the technology can drive a large current. The resulting load-driving capability is one reason for ECL's popularity.*




*4. In a deep-submicron CMOS device structure, drain current is increased by substantially decreasing gate length, $L_g$, and gate-oxide thickness, $t_{ox}$, thus increasing driving capability.*




*5. The driving capability of CMOS circuits has been improving steadily. The estimated driving capability of the 0.2-μm-gate CMOS is derived from the device characteristics for deep-submicron CMOS reported so far [1,2].*

circuits and devices. ECL has been favored because of its large driving capability; conventional CMOS is weak in this area.

Driving capability is directly proportional to signal current divided by the signal voltage. CMOS's signal voltage is as large as 5 V and its driving current is small. On the other hand, ECL can drive a large current and its signal voltage is as small as 0.5 V (Fig. 3).

But things are changing. The drain current of a CMOS device can be increased by decreasing gate length $L_g$ and gate-oxide thickness $t_{ox}$ (Fig. 4). A fairly large drain current has been reported at a drain voltage as low as 2 V when gate length is decreased to approximately 0.2 μm [1,2]. Such "deep-submicron" devices represent the latest in a steady stream of improvements in the driving capability of CMOS circuits (Fig. 5).

The driving capability of ECL circuits, on the other hand, is mainly determined by the current flowing through the emitter-follower pull-down resistor when the output signal changes from high to low. Therefore, the circuit's driving capability is determined primarily by power dissipation and cannot benefit from device miniaturization. Since ECL circuit power cannot be increased in the future, the driving capability of CMOS will be equivalent to that of ECL when deep-submicron devices become available. The driving capability of ECL may still be improved by adopting active pull-down circuit techniques, but CMOS is attractive because its device structure and circuit configuration are very simple.

The delay caused by long signal nets on printed circuit boards and module substrates often determines system performance. Driving such long nets has been a strong point of ECL. Usually, such signal nets are treated as controlled-impedance-terminated (CIT) nets, in which case signals reach the far end of the net with minimum delay. ECL is suitable for driving CIT nets.

In CMOS VLSI, long nets are implemented on the chip. Wire resistance is large, and resistance-capacitance (RC) nets are used. Delay per unit length of RC nets is larger than that of CIT nets, but wire length is shorter for CMOS VLSI so total delay can be competitive.

## Case Study

*Device Requirements and VLSI Chip Model*

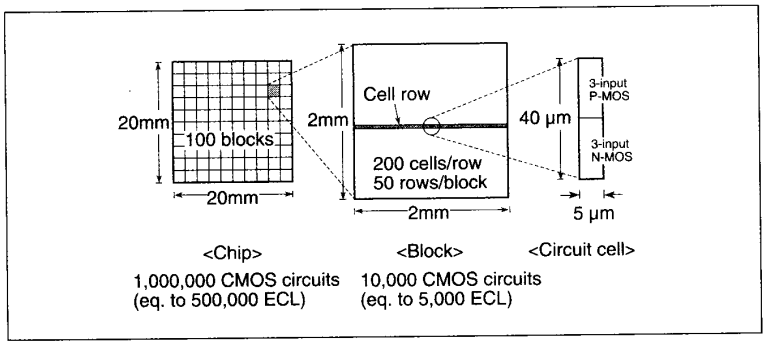
Based on our experience and the data reported so far, we expect certain basic characteristics for 0.2-μm gate-length, room-temperature CMOS (Table 3)[1,2]. To evaluate the possibilities of CMOS, we assume a particular VLSI chip model (Fig. 6). In actuality, almost half of the chip area will be occupied by memory circuits, but in this case study we assume that the chip consists of logic only. As a result, we are considering the worst-case wire length.

In the model, we assume a CMOS chip area of 20 mm x 20 mm, a reasonable assumption considering that a 15 mm x 15 mm ECL chip is used today [13]. The chip is hypothetically divided into 100 identical blocks. Actually, the block size will not be identical, especially when standard-cell design methodology is applied, but the assumption is valid for evaluating performance and chip area. Ten thousand CMOS circuits can be integrated in a 2-mm x 2-mm block. This leaves sufficient area for interblock buffers and chip input-output (I/O) circuits, because a 3-input CMOS NAND using 15-μm-gate-width FETs can

Table 4: Packaging Density of Future CMOS* VLSI Chips and Modern** ECL Modules

| | | Packaging density | Wire Length |
|---|---|---|---|
| 1st level | CMOS (block) | 1,250/mm² | |
| | ECL (chip) | 100/mm² | |
| | Ratio | 12.5 | 1/3.5 |
| 2nd level | CMOS (chip) | 125,000/cm² | |
| | ECL (module) | 4,000/cm² | |
| | Ratio | 30 | 1/5.5 |

*deep-submicron
**early 1990's




*6. A chip model for future CMOS VLSI computer logic.*

be placed in a 40 μm x 5 μm area when 0.3-μm lithography is used. We assume the gate width of 15 μm, which would be unreasonably large for a microprocessor design, to obtain a large driving capability equivalent to ECL.

In our model, one million CMOS circuits with large driving capability are implemented on a chip. The chip is equivalent to 500,000 ECL circuits in terms of its logic-function capabilities. Implementing the same logic by the most modern ECL technology would result in a much larger module (Fig. 7). Let's compare the packaging density and wire length of the ECL module with the CMOS VLSI (Table 4). Since the integration scale of a modern ECL chip is 5,000 to 20,000 gates [14], 25 to 100 ECL chips would be necessary.

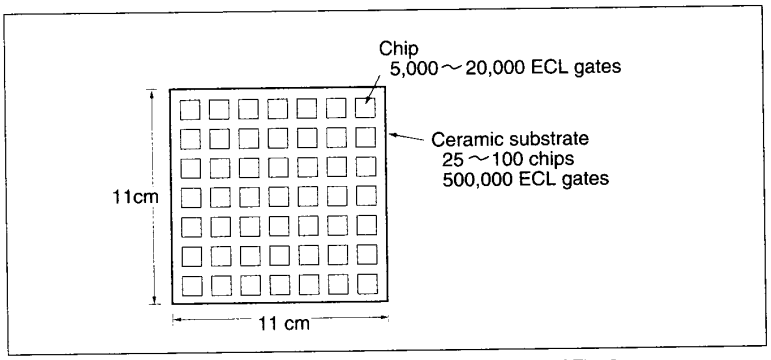
One CMOS block on the VLSI chip is equivalent to one ECL chip in terms of gate count. Since the density of the modern ECL is about 100 gate/mm$^2$ [15-17], the CMOS is 12.5 times denser. Therefore, the wire length of the CMOS is 1/3.5 that used in ECL. One CMOS chip is equivalent to one ECL module. Since the density of the modern ECL module is 3,500-4,000 gate/cm$^2$ [14], an 11 cm x 11 cm ceramic substrate is necessary. The CMOS is 30 times denser, and its wire length is 1/5.5 that used in ECL.

The estimated wire length of the CMOS VLSI chip is shown in Table 5 using the equations reported in [7]. A Rent's Rule coefficient of r = 2/3 is used. Two cases are shown for the intrablock nets. The first case (left column) assumes that CMOS circuits are uniformly distributed in the block, and applies to estimating total wire length. The second case (right column) applies when four CMOS circuits are used as a cluster to implement one ECL function, and applies to estimating critical path delay.

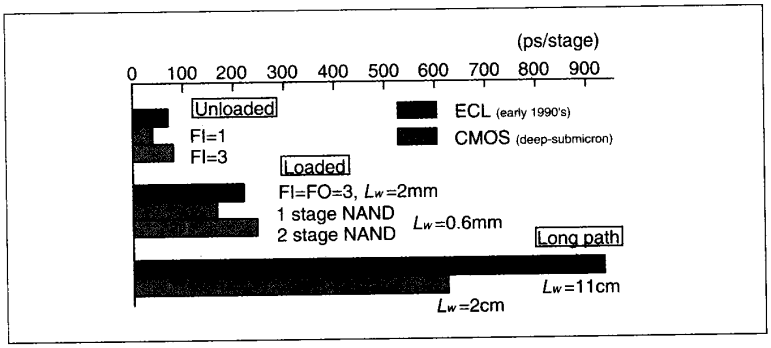
If the average number of terminal-to-terminal wires per signal net, $n_{pp}$, is 2, that is, FO = 2, wire length per signal net is about 240 μm for intrablock and 9 mm for interblock. Therefore, the total wire length in a block is about 2.4 m since each block has 10,000 signal nets. If wire channel pitch is 1.5 μm (that is, width = spacing = 0.75 μm), two signal layers are required for the intrablock wiring because approximately 50 percent of the total channel length is usable. As for the interblock wiring, the total wire length in a chip is about 100 m since the number of output terminals of a 5,000-ECL equivalent-circuit block is estimated to be 100 - 110. Since the interblock wire resistance causes a significant delay, a wire channel pitch as large as 6 μm is assumed for estimating performance. In this case, three signal layers are required for the interblock wiring. The required number of metal layers is at least six, including power and ground layers. This requirement is not easy to meet, but is not unrealistic for the future since 4-metal-layer chips are already used today [14].

*Delay and Power Consumption of the CMOS VLSI Chip*

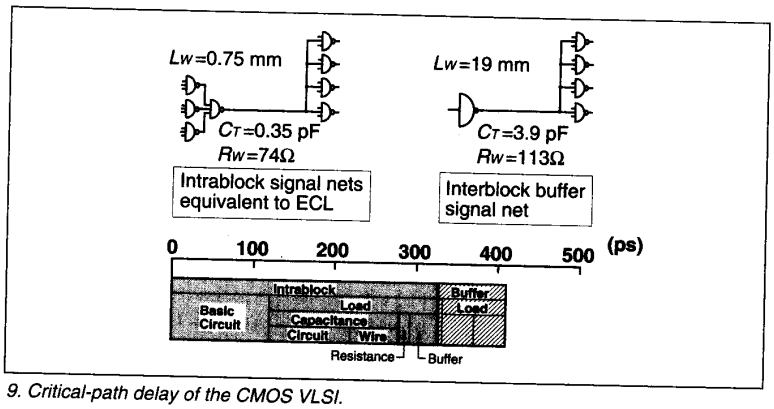
Let's compare the delays of the modern ECL and the deep-submicron CMOS (Fig. 8). The lightly-loaded circuit delay of ECL is 70 ps [14]. The corresponding delay of CMOS is 40 ps for a 1-input inverter and 80 ps for a 3-input NAND gate, as shown in Table 3. The delay of the ECL with 3 fan-outs and 2-mm wire is 220 ps [17]. The corresponding wire length for CMOS is 0.6 mm (from Table 4). Using Table 3, the delay of




*7. A hypothetical ECL module equivalent to the CMOS VLSI chip of Fig. 6.*




*8. Projected delays in deep-submicron CMOS VLSI.*




*9. Critical-path delay of the CMOS VLSI.*

the CMOS is estimated to be 170 ps for a 1-stage NAND. If a 2-stage circuit is needed to obtain logic-function capability equivalent to that of an ECL, the delay is 250 ps.

In the case of ECL, if a signal net is as long as one side of the module substrate, the transmission delay is about 800 ps because the dielectric constant of the substrate is 5.7 - 5.9 [14]. Assuming that the delay of a buffer circuit used for driving the wire is twice the lightly loaded circuit delay, the total delay of the net would be about 940 ps. The corresponding delay of the CMOS would be about 620 ps, assuming a buffer circuit consisting of two stages of inverters for driving the 2-cm wire. The gate widths of the transistors are 15 μm for the first stage and 75 μm for the second stage. The delay of the buffer circuit is estimated as 140 ps. The wire and load capacitance $C_T$ would cause a delay of 240 ps, and the delay caused by wire resistance RW is estimated as 240 ps ($0.5\ R_W C_T$).

Although a larger coefficient for the worst case should be assumed for CMOS than for ECL, delays of the CMOS are comparable to the ECL in the various paths in Fig. 8. These results indicate that system performance obtained by the deep-submicron CMOS will be roughly equivalent to the most modern ECL systems.

Various paths were used in the preceding comparison of ECL and CMOS delays, but a more comprehensive discussion of system performance requires a model of typical critical paths. Figure 9 shows one example of such models. The intrablock circuit model consists of two CMOS NAND stages with three inputs and four fan-outs for the second stage, which has associated wires. This is approximately equivalent to one ECL stage in critical paths. Total capacitance of this net is estimated to be 0.35 pF, using the wire length in Table 5 and the circuit characteristics in Table 3. The length of this wire is 0.75 mm and its resistance is 74 Ω. The net's total delay is about 290 ps.

Using interblock buffer circuits decreases the total delay in communicating with other blocks. The buffer circuit shown in Fig. 9 is a simple CMOS inverter with 75-μm-gate-width FETs. Fan-outs of four and associated wires are assumed. Total capacitance of this net is estimated as 3.9 pF, using the wire length in Table 5 and the circuit characteristics in Table 3. The length of this wire is 19 mm and its resistance is 113 Ω. This net's total delay is about 490 ps. Since the input capacitance of this circuit is large and the wire connecting the circuit with an intrablock circuit could be as long as 1 mm, an additional delay of about 200 ps should be assumed when driving this circuit with an intrablock circuit. Thus, total delay for the buffer circuit is estimated as 690 ps.

To obtain CMOS delays corresponding to ECL critical paths, a portion of the buffer delay has to be added to the intrablock delay. From the data reported in [18] the number of ECL equivalent circuit stages is estimated to be about six, considering that the block is equivalent to 5,000 ECL circuits. To obtain the "system delay," one sixth of the buffer-circuit delay should be added to the intrablock circuit delay.

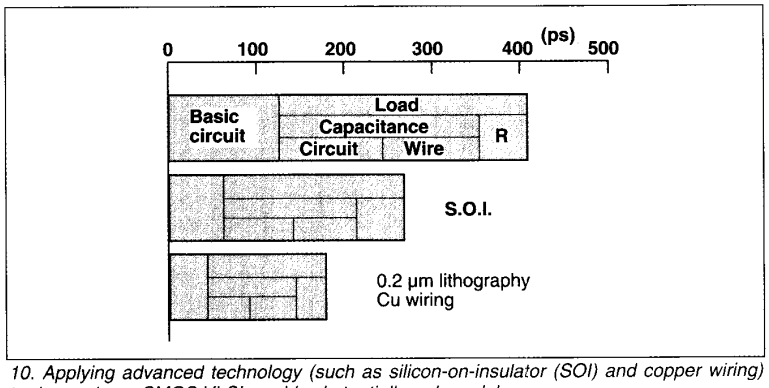
The delay is about 400 picoseconds under typical process parameters and system environments. Assuming a coefficient of 1.5 for the worst case, the value for estimating the system performance is about 600 ps. Since the chip integration is very large, almost all portions of the critical

Table 5. Estimated Wire Lengths – CMOS VLSI Chip

| | Intrablock | | Interblock |
|---|---|---|---|
| Circuits/cell | 1 | 4 | |
| Area (mm x mm) | 2 x 2 | 2 x 2 | 20 x 20 |
| No. of cells or blocks/area | 200 x 50 | 50 x 50 | 10 x 10 |
| Wire length *lpp* x *p* (μm) | 121 | 189 | 4,660 |
| Total wire length (mm) | 2,415 | | 97,860 |
| Channel pitch (μm) | 1.5 | | 6.0 |
| Number of layers required | 2 | | 3 |

Table 6. Estimated Device Parameters of the CMOS VLSI Chip

| | Intrablock | Interblock |
|---|---|---|
| Wire length/net (mm) | 0.24 | 9.3 |
| Fan-outs/net | 2 | 2 |
| Capacitance/net (pF) | | |
| Wire | 0.048 | 1.86 |
| Load Circuits | 0.10 | 0.10 |
| Net Total | 0.148 | 1.96 |
| Switching energy/net (pJ) | 0.94 | 8.4 |
| /chip (μJ) | 0.94 | 0.088 |
| Avg. Switching Period (ns) | 25 | 25 |
| Power/net (μW) | 38 | 340 |
| /chip (W) | 38 | 3.6 |




*10. Applying advanced technology (such as silicon-on-insulator (SOI) and copper wiring) to deep-micron CMOS VLSI would substantially reduce delays.*

paths can be implemented on one chip. The delay we've obtained can thus be directly compared to the system delay of ECL machines, which consists of on-chip circuit and loading delay, chip I/O delay, and wire delay on module substrates and/or printed circuit boards.

The switching period is estimated to be about 25 ns, using $k = 40$ and the system delay a little larger than 600 ps. The power of the CMOS chip can be estimated using the switching period, the device and basic circuit characteristics in Table 3, and the wire lengths in Table 5. As shown in Table 6, the total power of the intrablock circuits and interblock buffers are 38 W and 4 W, respectively. Total chip power will be about 50 W, including chip I/O circuits. If equivalent logic is implemented by using 2-mW ECL circuits, the total power would be more than 20 times larger.

**Discussion**

If the deep-submicron device in Table 3 is realized, we will be able to obtain system performance from CMOS computer-logic circuits equivalent to today's most modern ECL systems. In addition CMOS has other possibilities.

The effects of applying advanced process and device technology are shown in Fig. 10. The uppermost bar shows the delay breakdown of the CMOS VLSI described above. The second bar shows the effects of applying fully depleted silicon on insulator devices. Better device performance is obtainable by realizing fully depleted SOI MOSFETs [19, 20]. If basic circuit speed is doubled (at x 1.5 original drain current) using the same level of lithography, the system delay decreases by one third. If further miniaturization is realized and low-resistance material such as copper is used for wiring, the delay will decrease to less than one half of the uppermost bar.

In the case of CMOS, system performance increases almost directly with improvements in device performance. This should provide strong motivation for developing advanced deep-submicron devices, including the technologies we've mentioned. The development of such devices should increase the possibility that room-temperature CMOS will become the long-pursued post-ECL high-speed technology. **CD**

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